A

MAJOR PROJECT REPORT ON

EFFICIENT IMPLEMENTATION OF 6T FULL ADDER CIRCUIT WITH LOW POWER 2T XOR-XNOR LOGIC

Submitted in partial fulfilment of the requirement for the award of degree of

BACHELOR OF TECHNOLOGY

IN

ELECTRONICS AND COMMUNICATION ENGINEERING

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Kandlakoya(V), Medchal(M), Telangana – 501401

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CERTIFICATE

This is to certify that the major-project work entitled **"EFFICENT IMPLEMENTATION OF 6T FULL ADDER CIRCUIT WITH LOW POWER 2T XOR-XNOR LOGIC"** is being submitted **M.SUSHANTH REDDY** bearing Roll No:**218R1A04N1,M.GNANESHWAR** bearing Roll No: **218R1A04N2, M.PRAVEEN KUMAR** bearing Roll No:**218R1A04N3**, **MD.NASARUDDIN** bearing RollNo :**218R1A04N4** in B.Tech IV-I semester, Electronics and Communication Engineering is a record Bonafide work carried out during the academic year 2024-25. The results embodied in this report have not been submitted to any other University for the award of any degree.

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DECLARATION

We hereby declare that the major project entitled **"EFFICIENT IMPLEMENTATION OF 6T FULL ADDER CIRCUIT WITH LOW POWER 2T XOR-XNOR LOGIC"** is the work done by us in campus at **CMR ENGINEERING COLLEGE,** Kandlakoya during the academic year 2024-2025 and is submitted as major project in partial fulfilment of the requirements for the award of degree of **BACHELOR OF TECHNOLOGY** in **ELECTRONICS AND COMMUNICATION ENGINEERING FROM JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD.**

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ABSTRACT

Exclusive-NOR (XNOR)AND XOR gates are important in digital circuits. This paper proposes the novel design of 2T XOR-XNOR gate using pass transistor logic. The proposed circuit utilizes the least number of transistors and no complementary input signals is used. The design has been compared with earlier designed XOR-XNOR gates and a significant improvement in silicon area and power-delay product has been obtained against 3T XOR-XNOR gate. Instead of cascading two two-input XOR-XNOR gates, we design a new structure of three-input function on the transistor level in this paper.

A 6 transistor full adder has been designed using the proposed two-transistor XOR-XNOR gate. The performance has been investigated using 0.18μm Technology and evaluated by the comparison of the simulation result obtain from TSPICE. Power consumption and delay factors are the main design restrictions in the developing nanometer technology Schematics. The major component of an ALU, or Arithmetic logic unit, of a processor is the full adder. Therefore, altering the Full Adder's parameters in a significant way will directly affect the ALU's and then the Processor's parameters. The conclusion drawn from the parametric analysis of output noise, power consumption, and delay obtained from the proposed circuits will then be presented.

In conclusion, this introduces an innovative and highly efficient 2T XOR-XNOR gate using pass transistor logic, achieving significant advancements in PDP, power consumption, and silicon area. The elimination of complementary input signals reduces complexity and enhances performance. The integration of this XOR-XNOR gate into a six-transistor full adder further highlights its applicability in arithmetic operations, making it a strong candidate for modern low-power and high-speed digital systems. Future research can explore the implementation of the proposed design in larger digital architectures, extending its benefits to broader VLSI applications.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 OVERVIEW OF THE PROJECT

The project "Efficient Implementation of a 6T Full Adder Circuit with Low Power 2T XOR-XNOR Logic" focuses on designing a low-power, area-efficient full adder circuit using 6 transistors (6T) and 2-transistor (2T) XOR-XNOR gates. A full adder is a fundamental component in digital arithmetic circuits, performing the sum and carry-out operations for two input bits and a carry-in bit.

The main objective of the project is to reduce power consumption by utilizing 2T XOR XNOR gates, which are known for their minimal transistor count and lower power dissipation compared to traditional XOR implementations. These gates are designed using pass-transistor logic or complementary CMOS logic, which are ideal for low-voltage operation and energy-efficient designs.

The 6T full adder combines two 2T XOR-XNOR gates for the sum calculation and efficient AND/OR gates for the carry-out. This reduces the total transistor count while maintaining the functionality of a standard full adder. The low-power design is achieved by optimizing the voltage and transistor sizing, minimizing leakage and dynamic power consumption. It also involves performance analysis using simulation tools, comparing power, delay, and area metrics to conventional full adder designs, highlighting the advantages of low-power operation in VLSI systems.

The project involves the design and simulation of the 6T full adder circuit with low power 2T XOR-XNOR logic gates using industry-standard simulation tools. The proposed circuit is compared with traditional 6T full adder circuits in terms of power consumption, delay, and area. The results show that the proposed circuit achieves a significant reduction in power consumption, making it an attractive solution for low-power digital circuit design. The project also explores the use of 2T XOR-XNOR logic gates in the design of more complex digital circuits, such as multi-bit adders and subtractors, to further reduce power consumption and increase performance. The project has several key objectives, including the design and simulation of the 6T full adder circuit with low power 2T XOR-XNOR logic

gates, the evaluation of the proposed circuit's performance in terms of power consumption, delay, and area, and the exploration of the use of 2T XOR-XNOR logic gates in more complex digital circuits. The project also aims to demonstrate the feasibility and effectiveness of the proposed circuit in a wide range of digital applications, from mobile devices to high-performance computing systems. Overall, the project aims to contribute to the development of more efficient, reliable, and scalable digital systems by providing a novel and innovative solution for low-power digital circuit design.

The project is expected to have a significant impact on the field of digital circuit design, enabling the development of more efficient, reliable, and scalable digital systems. The proposed 6T full adder circuit with low power 2T XNOR logic gates has the potential to revolutionize the design of digital arithmetic circuits and enable the development of more complex digital systems with reduced power consumption and increased performance. The project's outcomes are expected to be of great interest to researchers, designers, and manufacturers of digital circuits and systems, and to contribute to the advancement of the field of digital circuit design.

1.2 OBJECTIVE OF THE PROJECT

The objective of the project "Efficient Implementation of a 6T Full Adder Circuit with Low Power 2T XOR-XNOR Logic" is to design a power-efficient and compact full adder circuit using 6 transistors (6T), leveraging 2-transistor (2T) XOR-XNOR gates for minimal power consumption. A full adder is a fundamental digital component used in arithmetic circuits for performing addition, specifically computing the sum and carry-out of two input bits and a carry-in bit. The project aims to optimize power dissipation by using 2T XOR-XNOR gates, which significantly reduce energy consumption compared to traditional XOR gates. These gates are based on pass-transistor logic or complementary CMOS, which provide low-voltage operation and reduced static and dynamic power.

By using 6 transistors, the full adder circuit reduces the transistor count compared to conventional designs, making it area-efficient and suitable for high-density VLSI applications. The design also focuses on minimizing delay and propagation time while maintaining optimal power performance, thus ensuring that the full adder meets the requirements of modern, energy-efficient digital systems. In addition, the project includes performance evaluation and comparison with traditional full adders, highlighting the

advantages of low-power design in areas such as mobile devices, embedded systems, and IoT applications.

1.3 ORGANIZATION OF THE PROJECT

The organization of the project "Efficient Implementation of a 6T Full Adder Circuit with Low Power 2T XOR-XNOR Logic" is structured to provide a comprehensive understanding of the design, analysis, and optimization of a low-power full adder circuit for VLSI applications. The Introduction chapter outlines the overview , objective of the project. Chapter 2 deals about Literature survey and Chapter 3 deals introduction to VLSI AND provides an overview of Tanner EDA, a powerful Electronic Design Automation (EDA) tool used for designing, simulating, and analyzing low-power VLSI circuits. It highlights the key features of Tanner EDA, including schematic design (S-Edit), SPICE simulation (T-Spice), and layout editing (L-Edit), and explains its importance in implementing the 6T full adder with low-power 2T XOR-XNOR logic.

Chapter-4 explores existing full adder architectures, analyzing their limitations in power, delay, and transistor count to justify the need for a more efficient 6T full adder with low-power 2T XOR-XNOR logic.AND it presents the proposed 6T full adder architecture using low-power 2T XOR-XNOR logic, emphasizing its advantages in power efficiency, reduced transistor count, and improved performance compared to existing designs. Chapter-5 presents the simulation results of the proposed 6T full adder using Tanner EDA, analyzing its power consumption, delay, and performance, and comparing it with existing architectures to demonstrate its efficiency and evaluates the performance of the proposed 6T full adder based on key metrics such as power, delay, and transistor count, with insights and validation from metrics to ensure design accuracy and efficiency.Chapter-6 discusses the advantages, disadvantages, applications, and conclusion of the proposed 6T full adder with 2T XOR-XNOR logic, highlighting its efficiency, challenges, and future potential in low-power digital systems**.**

CHAPTER 2
LITERATURE SURVEY

2.1 DESIGN OF LOW POWER FULL ADDER BASED WALLACE TREE MULTIPLIER USING CADENCE 180NM TECHNOLOGY

In recent year, power dissipation is one of the biggest challenges in VLSI Design. Multipliers are the main sources of power dissipation in DSP blocks. This project presents efficient 4-bits unsigned binary multipliers architectures, such as Array multiplier and Wallace Tree Multiplier. This implementation carried out using cadence 180nm technology. In This design, initially design transistor level schematic circuits than create the test symbol, multiplier circuits are efficiently optimized in terms of area and power.

The implementation consist of combinational components such as 1-bit Full Adders, AND, XOR, Half Adder, Inverter circuits. The circuit analysis is carried out in terms of performance parameter such as transistor count, and power consumption. According to the estimation done the transistor count and power consumption of array multiplier was found to be 288, 446.5µw respectively, for Wallace tree multiplier was found to be 262, 134.7µw.

2.2 A NEW DESIGN 6T FULL ADDER CIRCUIT USING NOVEL 2T XNOR GATES

Exclusive-NOR (XNOR) gates are important in digital circuits. This paper proposes the novel design of 2T XNOR gate using pass transistor logic. The proposed circuit utilizes the least number of transistors and no complementary input signal is used. The design has been compared with earlier designed XNOR gates and a significant improvement in silicon area and power-delay product has been obtained against 3T XNOR gate.

In this we designed a new 6 transistor full adder using the proposed two-transistor XNOR gate. The performance has been investigated using 0.18µm Technology and evaluated by the comparison of the simulation result obtain from TSPICE.

2.3 DESIGN OF LOW POWER AND HIGH SPEED FULL ADDER CELL USING NEW 3T XNOR GATE

In the current age of technology advancement it is necessary to design different new concepts to reduce area of the cell as well as power consumption. The adders are always meant to be the most fundamental requirements for process of high performance and other multi core devices. In present work a new XNOR gate using three transistors has been designed, which shows power dissipation of 0.03866W in 90nm technology with supply voltage of 1.2V. A single bit full adder using eight transistors has been designed using proposed XNOR cell and a multiplexer, which shows power dissipation of 0.07736W. It is implemented by using synopsys tool(version-L-2016.06-8) using custom compiler with 90nm technology.

2.4 A NOVEL HIGH-SPEED AND ENERGY EFfiCIENT10-TRANSISTOR FULL ADDER DESIGN

In this, we propose a novel full adder design using as few as ten transistors per bit. Compared with other low-gate-count full adder designs using pass transistor logic, the pro-posed design features lower operating voltage, higher computing speed and lower energy (power delay product) operation. The design adopts inverter buffered XOR/XNOR designs to alleviate the threshold voltage loss problem commonly encountered in pass transistor logic design. This problem usually prevents the full adder design from operating in low supply voltage or cascading directly without extra buffering.

The proposed design successfully embeds the buffering circuit in the full adder design and the transistor count is minimized. The improved buffering helps the design operate under lower supply voltage compared with existing works. It also enhances the speed performance of the cascaded operation significantly while maintaining the performance edge in energy consumption. For performance comparison, both dc and performances of the proposed design against various full adder designs are evaluated via extensive HSPICE simulations. The simulation results, based on TSMC 2P4M 0.35-m process models, indicate that the proposed design has the lowest working and highest working frequency among all designs using ten transistors. It also features the lowest energy consumption per addition among these designs. In addition, the performance edge of the proposed design in both speed and energy consumption becomes even more significant as the word length of the adder increases.

2.5 A STANDARD CELL BASED SYNCHRONOUS DUAL-BIT ADDER WITH EMBEDDED CARRY LOOK-AHEAD

A novel synchronous dual-bit adder design, realized using the elements of commercial standard cell libraries, is presented in this article. The adder embeds two-bit carry look-ahead generator functionality and is realized using simple and compound gates of the standard cell library. The performance of the proposed dual-bit adder design is evaluated and compared vis-à-vis the conventional full adder (implemented using two half adder blocks) and the library's full adder element, when performing 32-bit addition on the basis of the fundamental carry propagate adder topology. Based on experimentations targeting the best case process corner of the high-speed 130nm UMC CMOS cell library and the highest speed corner of the inherently power optimized 65nm STMicro electronics CMOS standard cell library, it has been found that the proposed adder module is effective in achieving significant performance gains even in comparison with the commercial library based adder whilst facilitating reduced energy-delay product.

CHAPTER 3
VLSI AND SOFTWARE REQUIREMENTS

3.1 INTRODUCTION TO VLSI

Very-Large-Scale Integration (VLSI) is a technology that allows the integration of thousands to millions of transistors onto a single chip, enabling the creation of highly complex digital circuits. VLSI has revolutionized the field of electronics, playing a critical role in the design of microprocessors, memory units, digital signal processors, and more. With the continuous advancement in semiconductor technology, VLSI circuits are now capable of achieving greater functionality while occupying less space, consuming lower power, and operating at higher speeds. These advancements make VLSI crucial for developing devices such as smartphones, computers, wearable technologies, and Internet of Things (IoT) systems.

In the context of VLSI projects, the goal is often to design, simulate, and implement digital or analog circuits using modern VLSI design methodologies. These projects typically involve the development of integrated circuits (ICs) with specific functionalities like arithmetic operations, data storage, signal processing, or communication tasks. Digital VLSI design focuses on the design of circuits that process binary data, such as adders, multiplexers, registers, and microprocessors. On the other hand, analog VLSI deals with continuous signals, often used in applications like amplifiers, oscillators, and filters.

VLSI (Very Large-Scale Integration) design is a process of designing integrated circuits (ICs) by integrating thousands, millions or even billions of transistors on a single chip. These ICs are used in a variety of electronic devices ranging from simple handheld devices to complex supercomputers. The history of VLSI design can be traced back to the 1950s when the first transistor was invented. Later on, in the 1960s, the first integrated circuit (IC) was developed which revolutionized the electronics industry. With the development of ICs, the size of electronic devices reduced drastically, and their functionality increased. In the 1970s, the first microprocessor was invented, which gave birth to the modern computer era. The 1980s saw the emergence of VLSI design as a discipline, and the first VLSI chip was designed in 1983. Since then, VLSI design has been advancing at a rapid pace, and the technology has evolved to produce more complex and efficient chips.

VLSI projects typically follow a design flow that includes several stages: specification, architecture design, logic design, physical design, and verification. In this process, designers use specialized tools like CAD software (e.g., Cadence, Synopsys, and Mentor Graphics) for simulation, layout, and verification to ensure that the design meets the required performance, power, and area constraints. Key challenges in VLSI design include optimizing the trade-offs between power, speed, and area, as well as addressing issues like noise, interconnect delays, and manufacturing limitations.

A typical VLSI project could range from the design of simple components like adders or multipliers to complex systems such as microprocessors or custom ICs for specific applications. The advent of low-power design techniques and energy-efficient systems has made low-power VLSI design a crucial area of research, especially for mobile and embedded applications.

In summary, VLSI projects play a fundamental role in the development of advanced electronic systems, pushing the boundaries of what is possible in terms of circuit complexity, size, and performance. These projects help bridge the gap between theoretical concepts in electronics and their practical implementation in real-world systems.

3.2 VLSI TECHNOLOGY

VLSI Design presents state-of-the-art papers in VLSI design, computer-aided design, design analysis, design implementation, simulation and testing. Its scope also includes papers that address technical trends, pressing issues, and educational aspects in VLSI Design. The Journal provides a dynamic high-quality international forum for original papers and tutorials by academic, industrial, and other scholarly contributors in VLSI Design.

The development of microelectronics spans a time which is even lesser than the average life expectancy of a human, and yet it has seen as many as four generations. Early 60’s saw the low density fabrication processes classified under Small Scale Integration (SSI) in which transistor count was limited to about 10. This rapidly gave way to Medium Scale Integration in the late 60’s when around 100 transistors could be placed on a single chip.

It was the time when the cost of research began to decline and private firms started entering the competition in contrast to the earlier years where the main burden was borne by the military. Transistor-Transistor logic (TTL) offering higher integration densities outlasted

other IC families like ECL and became the basis of the first integrated circuit revolution. It was the production of this family that gave impetus to semiconductor giants like Texas Instruments, Fairchild and National Semiconductors. Early seventies marked the growth of transistor count to about 1000 per chip called the Large Scale Integration.

By mid-eighties, the transistor count on a single chip had already exceeded 1000 and hence came the age of Very Large Scale Integration or VLSI. Though many improvements have been made and the transistor count is still rising, further names of generations like ULSI are generally avoided. It was during this time when TTL lost the battle to MOS family owing to the same problems that had pushed vacuum tubes into negligence, power dissipation and the limit it imposed on the number of gates that could be placed on a single die.

The second age of Integrated Circuits revolution started with the introduction of the first microprocessor, the 4004 by Intel in 1972 and the 8080 in 1974. Today many companies like Texas Instruments, Infineon, Alliance Semiconductors, Cadence, Synopsys, Celox Networks, Cisco, Micron Tech, National Semiconductors, ST Microelectronics, Qualcomm, Lucent, Mentor Graphics, Analog Devices, Intel, Philips, Motorola and many other firms have been established and are dedicated to the various fields in "VLSI" like Programmable Logic Devices, Hardware Descriptive Languages, Design tools, Embedded Systems etc.

In 1980s, hold-over from outdated taxonomy for integration levels. Obviously, influenced from frequency bands, i.e., HF, VHF, and UHF. Sources disagree on what is measured (gates or transistors)

SSI – Small-Scale Integration (0-102)

MSI – Medium-Scale Integration (102 -103)

LSI – Large-Scale Integration (103 -105)

VLSI – Very Large-Scale Integration (105 - 107)

ULSI – Ultra Large-Scale Integration (>= 107)

VLSI Technology, Inc. was a company which designed and manufactured custom and semi-custom ICs. The company was based in Silicon Valley, with headquarters at 1109 McKay Drive in San Jose, California. Along with LSI Logic, VLSI Technology defined the leading edge of the application-specific integrated circuit (ASIC) business, which accelerated the push of powerful embedded systems into affordable products. The company was founded in 1979 by a trio from Fairchild Semiconductor by way of Synertek - Jack

Balletto, Dan Floyd, and Gunnar Wetlesen - and by Doug Fairbairn of Xerox PARC and Lambda (later VLSI Design) magazine.

Alfred J. Stein became the CEO of the company in 1982. Subsequently VLSI built its first fab in San Jose; eventually a second fab was built in San Antonio, Texas. VLSI had its initial public offering in 1983, and was listed on the stock market as (NASDAQ: VLSI). The company was later acquired by Philips and survives to this day as part of NXP Semiconductors.

The first semiconductor chips held two transistors each. Subsequent advances added more and more transistors, and, as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device. Now, known retrospectively as small-scale integration (SSI), improvements in technique led to devices with hundreds of logic gates, known as medium-scale integration (MSI).

Further improvements led to large-scale integration (LSI), i.e. systems with at least a thousand logic gates. Current technology has moved far past this mark and today's microprocessors have many millions of gates and billions of individual transistors.

At one time, there was an effort to name and calibrate various levels of large-scale integration above VLSI. Terms like ultra-large-scale integration (ULSI) were used. But the huge number of gates and transistors available on common devices has rendered such fine distinctions moot. Terms suggesting greater than VLSI levels of integration are no longer in widespread use.As of early 2008, billion-transistor processors are commercially available. This is expected to become more commonplace as semiconductor fabrication moves from the current generation of 65 nm processes to the next 45 nm generations (while experiencing new challenges such as increased variation across process corners).

A notable example is NVidia’s 280 series GPU. This GPU is unique in the fact that almost all of its 1.4 billion transistors are used for logic, in contrast to the Itanium, whose large transistor count is largely due to its 24 MB L3 cache. Current designs, as opposed to the earliest devices, use extensive design automation and automated logic synthesis to lay out the transistors, enabling higher levels of complexity in the resulting logic functionality. Certain high-performance logic blocks like the SRAM (Static Random Access Memory)

cell, however, are still designed by hand to ensure the highest efficiency (sometimes by bending or breaking established design rules to obtain the last bit of performance by trading stability).VLSI technology is moving towards radical level miniaturization with introduction of NEMS technology. A lot of problems need to be sorted out before the transition is actually made.

3.3 WHY VLSI?

Integration improves the design, lowers the parasitics, which means higher speed and lower power consumption and physically smaller. The Integration reduces manufacturing cost - (almost) no manual assembly.

The course will cover basic theory and techniques of digital VLSI design in CMOS technology. Topics include: CMOS devices and circuits, fabrication processes, static and dynamic logic structures, chip layout, simulation and testing, low power techniques, design tools and methodologies, VLSI architecture. We use full-custom techniques to design basic cells and regular structures such as data-path and memory.

There is an emphasis on modern design issues in interconnect and clocking. We will also use several case-studies to explore recent real-world VLSI designs (e.g. Pentium, Alpha, PowerPC Strong ARM, etc.) and papers from the recent research literature. On-campus students will design small test circuits using various CAD tools. Circuits will be verified and analyzed for performance with various simulators. Some final project designs will be fabricated and returned to students the following semester for testing.

Very-large-scale integration (VLSI) is the process of creating integrated circuits by combining thousands of transistor-based circuits into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. The term is no longer as common as it once was, as chips have increased in complexity into the hundreds of millions of transistors.

The first semiconductor chips held one transistor each. Subsequent advances added more and more transistors, and, as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device.

Now known retrospectively as "small-scale integration" (SSI), improvements in technique led to devices with hundreds of logic gates, known as large-scale integration (LSI), i.e. systems with at least a thousand logic gates. Current technology has moved far past this mark and today's microprocessors have many millions of gates and hundreds of millions of individual transistors.

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As of early 2008, billion-transistor processors are commercially available, an example of which is Intel's Montecito Itanium chip. This is expected to become more commonplace as semiconductor fabrication moves from the current generation of 65 nm processes to the next 45 nm generations (while experiencing new challenges such as increased variation across process corners). Another notable example is NVIDIA’s 280 series GPU.

This microprocessor is unique in the fact that its 1.4 Billion transistor count, capable of a teraflop of performance, is almost entirely dedicated to logic (Itanium's transistor count is largely due to the 24MB L3 cache). Current designs, as opposed to the earliest devices, use extensive design automation and automated logic synthesis to lay out the transistors, enabling higher levels of complexity in the resulting logic functionality. Certain high-performance logic blocks like the SRAM cell, however, are still designed by hand to ensure the highest efficiency (sometimes by bending or breaking established design rules to obtain the last bit of performance by trading stability).

The original business plan was to be a contract wafer fabrication company, but the venture investors wanted the company to develop IC (Integrated Circuit) design tools to help fill the foundry. Thanks to its Caltech and UC Berkeley students, VLSI was an important pioneer in the electronic design automation industry. It offered a sophisticated package of tools, originally based on the 'lambda-based' design style advocated by Carver Mead and Lynn Conway. VLSI became an early vendor of standard cell (cell-based technology) to the merchant market in the early 80s where the other ASIC-focused company, LSI Logic, was a

leader in gate arrays. Prior to VLSI's cell-based offering, the technology had been primarily available only within large vertically integrated companies with semiconductor units such as AT&T and IBM.VLSI's design tools eventually included not only design entry and simulation but eventually cell-based routing (chip compiler), a datapath compiler, SRAM and ROM compilers and a state machine compiler.

The tools were an integrated design solution for IC design and not just point tools, or more general purpose system tools. A designer could edit transistor-level polygons and/or logic schematics, then run DRC and LVS, extract parasites from the layout and run Spice simulation, then back-annotate the timing or gate size changes into the logic schematic database. Characterization tools were integrated to generate Frame Maker Data Sheets for Libraries. VLSI eventually spun off the CAD and Library operation into Compass Design Automation but it never reached IPO before it was purchased by Avanti Corp.

VLSI's physical design tools were critical not only to its ASIC business, but also in setting the bar for the commercial EDA industry. When VLSI and its main ASIC competitor, LSI Logic, were establishing the ASIC industry, commercially-available tools could not deliver the productivity necessary to support the physical design of hundreds of ASIC designs each year without the deployment of a substantial number of layout engineers. The companies' development of automated layout tools was a rational "make because there's nothing to buy" decision. The EDA industry finally caught up in the late 1980s when Tangent Systems released its TanCell and TanGate products. In 1989, Tangent was acquired by Cadence Design Systems (founded in 1988).

Unfortunately, for all VLSI's initial competence in design tools, they were not leaders in semiconductor manufacturing technology. VLSI had not been timely in developing a 1.0 µm manufacturing process as the rest of the industry moved to that geometry in the late 80s. VLSI entered a long-term technology partnership with Hitachi and finally released a 1.0 µm process and cell library (actually more of a 1.2 µm library with a 1.0 µm gate).

As VLSI struggled to gain parity with the rest of the industry in semiconductor technology, the design flow was moving rapidly to a Verilog HDL and synthesis flow. Cadence acquired Gateway, the leader in Verilog hardware design language (HDL) and Synopsys was dominating the exploding field of design synthesis. As VLSI's tools were being eclipsed, VLSI waited too long to open the tools up to other fabrications and Compass.

Design Automation was never a viable competitor to industry leaders. Meanwhile, VLSI entered the merchant high speed static RAM (SRAM) market as they needed a product to drive the semiconductor process technology development. All the large semiconductor companies built high speed SRAMs with cost structures VLSI could never match. VLSI withdrew once it was clear that the Hitachi process technology partnership was working .ARM Ltd was formed in 1990 as a semiconductor intellectual property licensor, backed by Acorn, Apple and VLSI.

VLSI became a licensee of the powerful ARM processor and ARM finally funded processor tools. Initial adoption of the ARM processor was slow. Few applications could justify the overhead of an embedded 32 bit processor. In fact, despite the addition of further licensees, the ARM processor enjoyed little market success until they developed the novel 'thumb' extensions. Ericsson adopted the ARM processor in a VLSI chipset for its GSM handset designs in the early 1990s. It was the GSM boost that is the foundation of ARM the company/technology that it is today. Only in PC chipsets, did VLSI dominate in the early 90s. This product was developed by five engineers using the 'Mega cells" in the VLSI library that led to a business unit at VLSI that almost equal its ASIC business in revenue. VLSI eventually ceded the market to Intel because Intel was able to package-sell its processors, chipsets, and even board level products together.

VLSI also had an early partnership with PMC, a design group that had been nurtured of British Columbia Bell. When PMC wanted to divest its semiconductor intellectual property venture, VLSI's bid was beaten by a creative deal by Sierra Semiconductor. The telecom business unit management at VLSI opted to go it alone. PMC Sierra became one of the most important telecom ASSP vendors. Scientists and innovations from the 'design technology' part of VLSI found their way to Cadence Design Systems (by way of Redwood Design Automation). Compass Design Automation (VLSI's CAD and Library spin-off) was sold to Avant! Corporation, which itself was acquired by Synopsys.

3.4 STRUCTURED DESIGN

Structured VLSI design is a modular methodology originated by Carver Mead and Lynn Conway for saving microchip area by minimizing the interconnect fabrics area. This is obtained by repetitive arrangement of rectangular macro blocks which can be interconnected using wiring by abutment.

An example is partitioning the layout of an adder into a row of equal bit slices cells. In complex designs this structuring may be achieved by hierarchical nesting.Structured VLSI design had been popular in the early 1980s, but lost its popularity later because of the advent of placement and routing tools wasting a lot of area by routing, which is tolerated because of the progress of Moore's Law. When introducing the hardware description language KARL in the mid' 1970s, Reiner Hartenstein coined the term "structured VLSI design" (originally as "structured LSI design"), echoing Edsger Dijkstra's structured programming approach by procedure nesting to avoid chaotic spaghetti-structured programs.

3.5 APPLICATIONS OF VLSI

- Electronic system in cars.
- Digital electronics control VCRs
- Transaction processing system, ATM
- Personal computers and Workstations
- Medical electronic systems.

Electronic systems now perform a wide variety of tasks in daily life. Electronic systems in some cases have replaced mechanisms that operated mechanically, hydraulically, or by other means; electronics are usually smaller, more flexible, and easier to service. In other cases electronic systems have created totally new applications. Electronic systems perform a variety of tasks; some of them are visible while some are hidden.

Personal entertainment systems such as portable MP3 players and DVD players perform sophisticated algorithms with remarkably little energy. Electronic systems in cars operate stereo systems and displays; they also control fuel injection systems, adjust suspensions to varying terrain, and perform the control functions required for anti-lock braking systems.

Digital electronics compress and decompress video, even at high-definition data rates, on-the-fly in consumer electronics. Low-cost terminals for Web browsing still require sophisticated electronics, despite their dedicated function. Personal computers and workstations provide word-processing, financial analysis, and games. Computers include both central processing units and special-purpose hardware for disk access, faster screen display, etc.

Medical electronic systems measure bodily functions and perform complex processing algorithms to warn about unusual conditions. The availability of these complex systems, far from overwhelming consumers, only creates demand for even more complex systems.

The growing sophistication of applications continually pushes the design and manufacturing of integrated circuits and electronic systems to new levels of complexity. And perhaps the most amazing characteristic of this collection of systems is its variety-as systems become more complex, we build not a few general-purpose computers but an ever wider range of special-purpose systems.

Our ability to do so is a testament to our growing mastery of both integrated circuit manufacturing and design, but the increasing demands of customers continue to test the limits of design and manufacturing.

3.6 ASIC

An Application-Specific Integrated Circuit (ASIC) is an integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use. For example, a chip designed solely to run a cell phone is an ASIC. Intermediate between ASICs and industry standard integrated circuits, like the 7400 or the 4000 series, are application specific standard products (ASSPs).

As feature sizes have shrunk and design tools improved over the years, the maximum complexity (and hence functionality) possible in an ASIC has grown from 5,000 gates to over 100 million. Modern ASICs often include entire 32-bit processors, memory blocks including ROM, RAM, EEPROM, Flash and other large building blocks. Such an ASIC is often termed a SoC (system-on-a-chip). Designers of digital ASICs use a hardware description language (HDL), such as Verilog or VHDL, to describe the functionality of ASICs.

Field-programmable gate arrays (FPGA) are the modern-day technology for building a breadboard or prototype from standard parts; programmable logic blocks and programmable interconnects allow the same FPGA to be used in many different applications. For smaller designs and/or lower production volumes, FPGAs may be more cost effective than an ASIC design even in production.

An application-specific integrated circuit (ASIC) is an integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use.

- A Structured ASIC falls between an FPGA and a Standard Cell-based ASIC
- Structured ASIC's are used mainly for mid-volume level designs
- The design task for structured ASIC's is to map the circuit into a fixed arrangement of known cells.

3.7 ASIC DESIGN FLOW

As with any other technical activity, development of an ASIC starts with an idea and takes tangible shape through the stages of development as shown in Fig 3.1 and in Fig 3.2. The first step in this process is to expand the idea in terms of behavior of the target circuit.

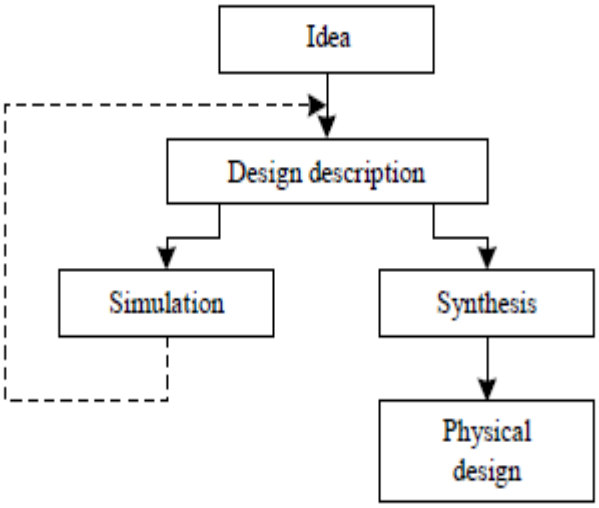


Fig:3.1 ASIC FLOW CHART

It is to check, verify, and ensure that what is wanted is what is described. Simulation is carried out through dedicated tools. With every simulation run, the simulation results are studied to identify errors in the design description. The errors are corrected and another simulation run carried out.

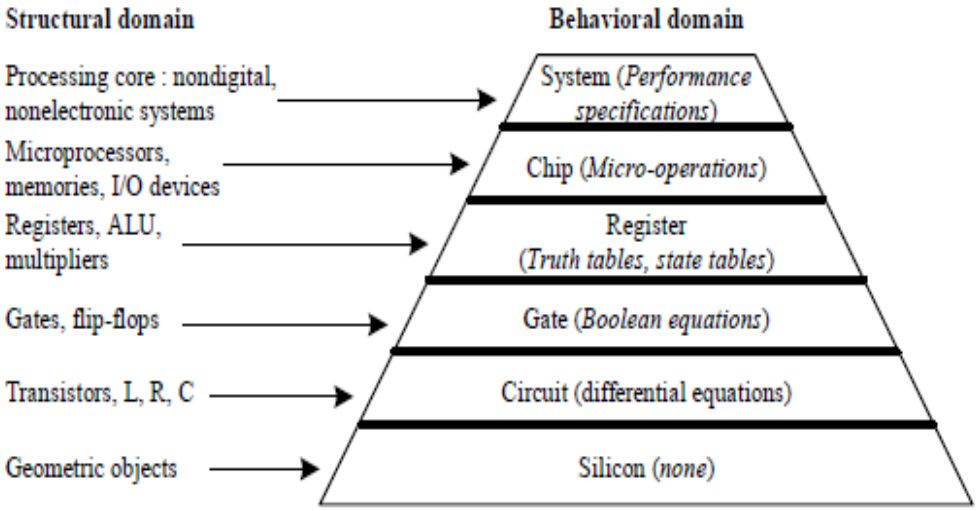


Fig :3.2 ASIC DESIGN FLOW

The design is tested through a simulation process; it is to check, verify, and ensure that what is wanted is what is described. Simulation is carried out through dedicated tools. With every simulation run, the simulation results are studied to identify errors in the design description. The errors are corrected and another simulation run carried out. Simulation and changes to design description together form a cyclic iterative process, repeated until an error-free design is evolved.

Design description is an activity independent of the target technology or manufacturer. It results in a description of the digital circuit. To translate it into a tangible circuit, one goes through the physical design process. The same constitutes a set of activities closely linked to the manufacturer and the target technology. It is to check, verify, and ensure that what is wanted is what is described. Simulation is carried out through dedicated tools. With every simulation run, the simulation results are studied to identify errors in the design description. The errors are corrected and another simulation run carried out.

3.8 STEPS IN THE VLSI DESIGN PROCESS

The different steps in the embedded system design flow/flow diagram include thefollowing.

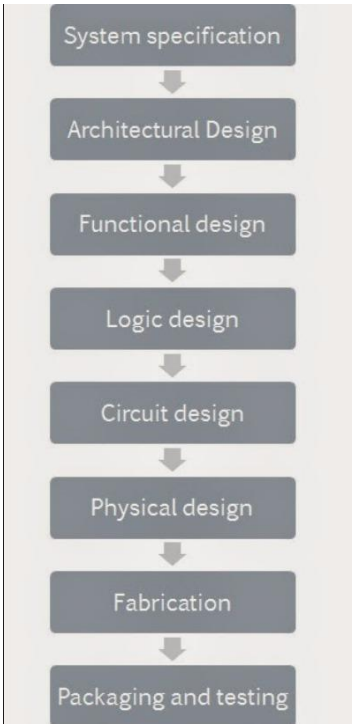


FIG:3.3. VLSI -PROCESS-STEPS

System Specification

The first step of any design process is to lay down the specifications of the system. System specification is a high level representation of the system. The factors to be considered in this process include: performance, functionality, and physical dimensions . The fabrication technology and design techniques are also considered.

Architectural Design

The basic architecture of the system is designed in this step. This includes, such decisions as RISC (Reduced Instruction Set Computer) versus CISC (Complex Instruction Set Computer), number of ALUs, Floating Point units, number and structure of pipelines, and size of caches among others.

Functional Design

In this step, main functional units of the system are identified. This also identifies the interconnect requirements between the units. The area, power, and other parameters of each unit are estimated.

Logic Design

In this step the control flow, word widths, register allocation, arithmetic operations, and logic operations of the that represent the functional design are derived and tested.

Circuit Design

The purpose of circuit design is to develop a circuit representation based on the logic design. The Boolean expressions are converted into a circuit representation by taking into consideration the speed and power requirements of the original design. Circuit Simulation is used to verify the correctness and timing of each component.

Physical Design

In this step the circuit representation (or netlist) is converted into a geometric representation. As stated earlier, this geometric representation of a circuit is called a layout. Layout is created by converting each logic component into a geometric representation , which perform the intended logic function of the corresponding component. Connections between different components are also expressed as geometric patterns typically lines in multiple layers.

Fabrication

After layout and verification, the design is ready for fabrication. Since layout data is typically sent to fabrication on a tape, the event of release of data is called Tape Out. Layout data is converted into photo-lithographic masks, one for each layer. Masks identify spaces on the wafer, where certain materials need to be deposited, diffused or even removed. Silicon crystals are grown and sliced to produce wafers.

Extremely small dimensions of VLSI devices require that the wafers be polished to near perfection. The fabrication process consists of several steps involving deposition, and diffusion of various materials on the wafer. During each step one mask is used. Several dozen masks may be used to complete the fabrication process.

Packing And Testing

Finally, the wafer is fabricated and diced into individual chips in a fabrication facility. Each chip is then packaged and tested to ensure that it meets all the design specifications and that it functions properly. Chips used in Printed Circuit Boards (PCBs) are packaged in Dual In-line Package (DIP), Pin Grid Array (PGA), Ball Grid Array (BGA), and Quad Flat Package (QFP). Chips used in Multi-Chip Modules (MCM) are not packaged, since MCMs use bare or naked chips.

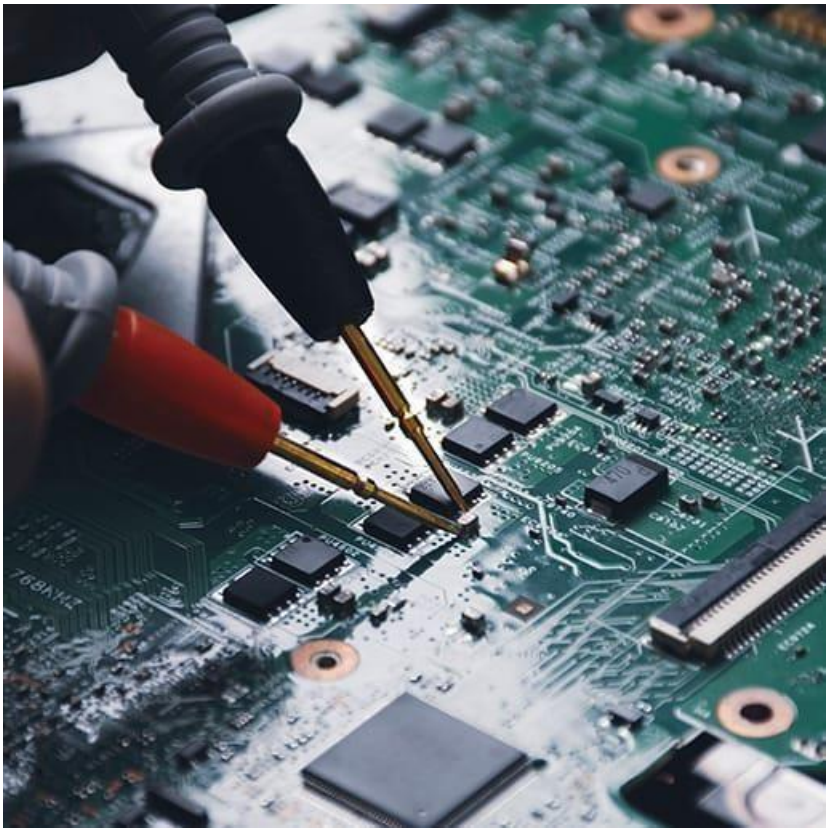


Fig:3.4 VLSI CHIP HARDWARE

VLSI is used in a variety of technologies across industries. Some examples include:

Computing and Information Technology: VLSI is the backbone of modern computing, enabling the development of powerful processors, memory chips, and graphics processing units (GPUs). It has driven the evolution of personal computers, laptops, smartphones, and data centers, which are essential for various applications, including artificial intelligence, cloud computing, and the Internet of Things (IoT).

Telecommunications: VLSI is used in the design and manufacturing of telecommunications equipment, such as routers, switches, and network processors, which facilitate high-speed data transmission and communication networks.

Consumer Electronics: VLSI is used in the development of various consumer electronics, including smartphones, tablets, smart TVs, and gaming consoles, which rely on complex integrated circuits to deliver high-performance and low-power consumption.

Automotive Electronics: VLSI is used in the design of advanced driver-assistance systems (ADAS), such as lane departure warning systems, adaptive cruise control, and automatic emergency braking, which rely on sophisticated sensors and processing units.

Medical Devices: VLSI is used in the development of medical devices, such as MRI and CT scanners, which require high-performance processing and imaging capabilities to produce detailed images of the human body.

Aerospace and Defense: VLSI is used in the design of complex electronic systems for military and aerospace applications, including radar systems, communication systems, and navigation systems.

Internet of Things (IoT): VLSI is used in the development of IoT devices, such as smart home appliances, wearables, and industrial sensors, which require low-power consumption and high-performance processing capabilities.

Artificial Intelligence (AI) and Machine Learning (ML): VLSI is used in the design of specialized AI and ML accelerators, such as graphics processing units (GPUs) and tensor processing units (TPUs), which enable fast and efficient processing of complex algorithms

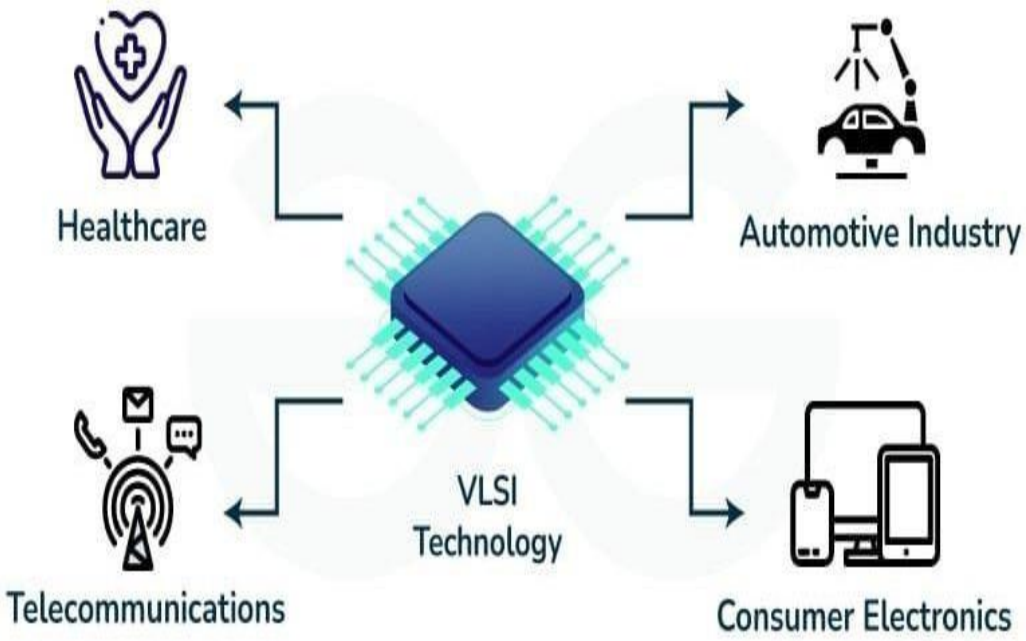


FIG:3.5 APPLICATIONS OF VLSI

3.9 SOFTWARE REQUIREMENTS :-TANNER EDA

SOFTWARE REQUIREMENTS: Tanner EDA v14.0 Software

3.9 THEORY:

Tanner tool is a Spice Computer Analysis Programmed for Analogue Integrated Circuits. Tanner tool consists of the following Engine Machines:

1. S-EDIT (Schematic Edit)
2. T-EDIT (Simulation Edit)
3. W-EDIT (Waveforms Edit)
4. L-EDIT (Layout Edit)
5. LVS (Layout Vs. Schematics)

Using these engine tools, spice program provides facility to the use to design & simulate new ideas in Analogue Integrated Circuits before going to the time consuming & costly process of chip fabrication.

3.9.1 -EDIT (SCHEMATIC EDIT)

S-Edit is hierarchy of files, modules & pages. It introduces symbol & schematic modes. S-Editprovides the facility of:

1. Beginning a design.
2. Viewing, drawing & editing of objects.
3. Design connectivity.
4. Properties, net lists & simulation.
5. Instance & browse schematic & symbol mode.

S-Edit has two viewing modes:

1.Schematic Mode: To create or view a schematic, we operate in schematic mode.

2.Symbol Mode: It represents symbol of a larger functional unit such as operational amplifier.

3.9.2 T-SPICE PRO CIRCUIT ANALYSIS

An introduction to the integrated components of the T- Spice Pro circuit analysis suite:

Schematic data files (.sdb): describes the circuits to be analyzed in graphical form, for display and editing by S- Edit" Schematic Editor.

Simulation input files (.sp): describes the circuits to be analyzed in textual form, for editing and simulation by T- Spice" Circuit Simulator.

Simulation output files (.out): containing the numerical results of the circuit analyses, for manipulation and display by W- Edit" Waveform Viewer.

3.9.3 CIRCUIT SIMULATOR (T-SPICE)

T-Spice Pro's waveform probing feature integrates S- Edit, T- Spice, and W- Edit to allow individual points in a circuit to be specified and analyzed. A few analyses are described below :The heart of T-Spice operation is the input file (also known as the circuit description, the net list &the input deck). This is a plain text file that contains the device statement & simulation commands, drawn from the SPICE circuit description language with which T-Spice constructs a model of the circuit to be simulated. Input files can be created and modified with any text editor. T-Spice is a tool used for simulation of the circuit. It provides the facility of

1. Design Simulation
2. Simulation Commands
3. Device Statements
4. User-Designed External Models
5. Small Signal & Noise Models

3.9.4 WAVEFORMS EDIT

The ability to visualize the complex numerical data resulting from VLSI circuit simulation is critical to testing, understanding & improving these circuits. W-Edit is a waveform viewer that provides ease of use, power & speed in a flexible environment designed for graphical data representation. The advantages of W-Edit include:

Tight Integration with T-spice, Tanner EDA_s circuit level simulator. W-Edit can chart data generated by T-spice directly, without modification of the output text data files. The

data can also be charted dynamically as it is produced during the simulation.Charts can automatically configure for the type of data being presented.

A data is treated by W-Edit as a unit called a trace. Multiple traces from different output files can be viewed simultaneously in single or several windows; traces can be copied and moved between charts & windows. Trace arithmetic can be performed on existed tracing to create new ones.Chart views can be panned back & forth and zoomed in & out, including specifying the exact X-Y co-ordinate range.Properties of axes, traces, rides, charts, text & colors can be customized.

3.9.5 LAYOUT(L-EDIT)

It is a tool that represents the masks that are used to fabricate an integrated circuit. It describes a layout design in terms of files, cells & mask primitives. On the layout level, the component parameters are totally different from schematic level. So it provides the facility to the user to analyze the response of the circuit before forwarding it to the time consuming & costly process of fabrication. There are rules for designing layout diagram of a schematic circuit using which user can compare the output response with the expected one.

3.10 STEPS TO MAKE A DESIGN USING TANNER TOOL

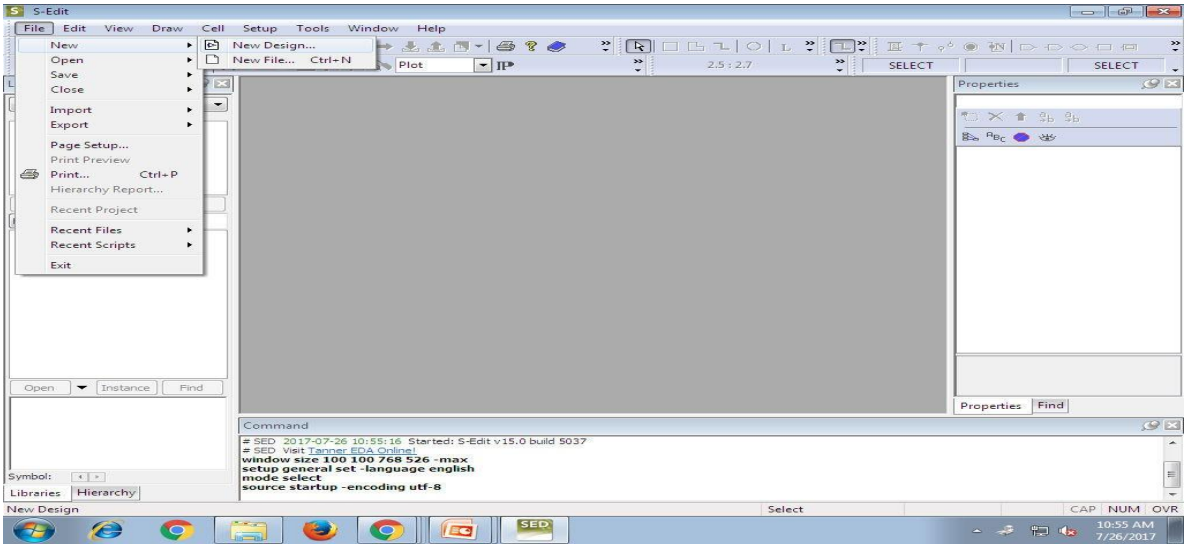
Opening S-edit platform:

First of all double click on the icon of s-edit on the desktop.
Or Go to the start menu >>All Programs >>Tanner EDA >>Tanner Tool v 14.0 >> S-Edit v 14.0.

Open new window.

Go to >>file >> New >> New Design

Select New Design

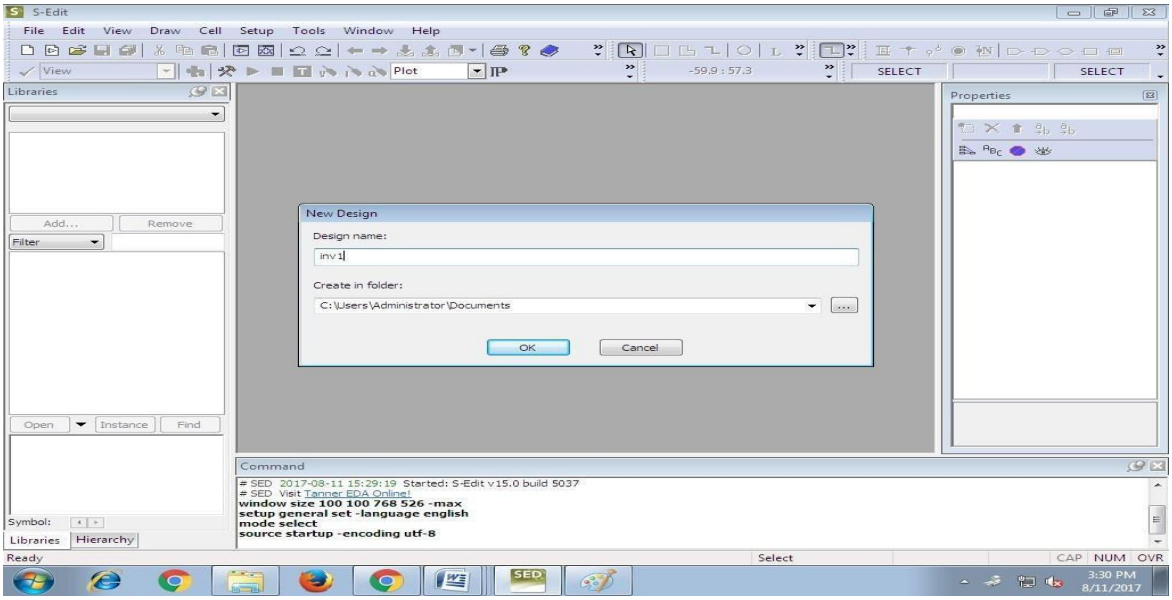


One dialog box will appear

Design Name : Give the name your design as you wish

Create a Folder: Give the path where you want to save the S-Edit Files.

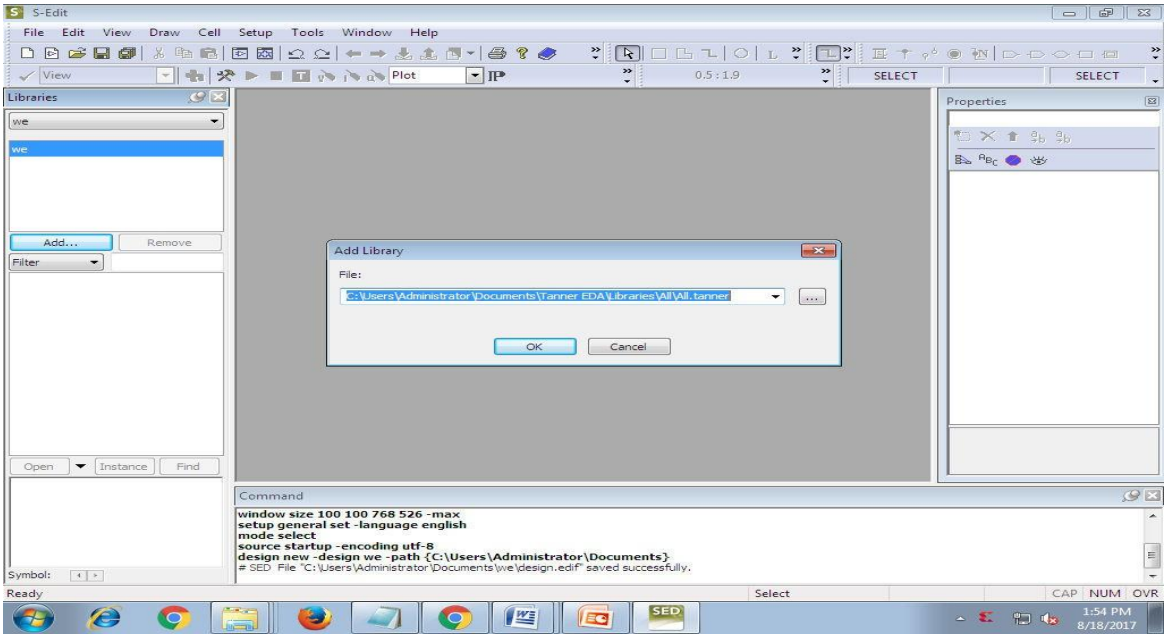
Then Click on ‘OK’.



Now to add libraries in your work click on “Add” left on the library window.

Give the path where Libraries are stored. As for example

C:\Users\Administrator\Documents\Tanner EDA\Libraries\All\All.tanner.

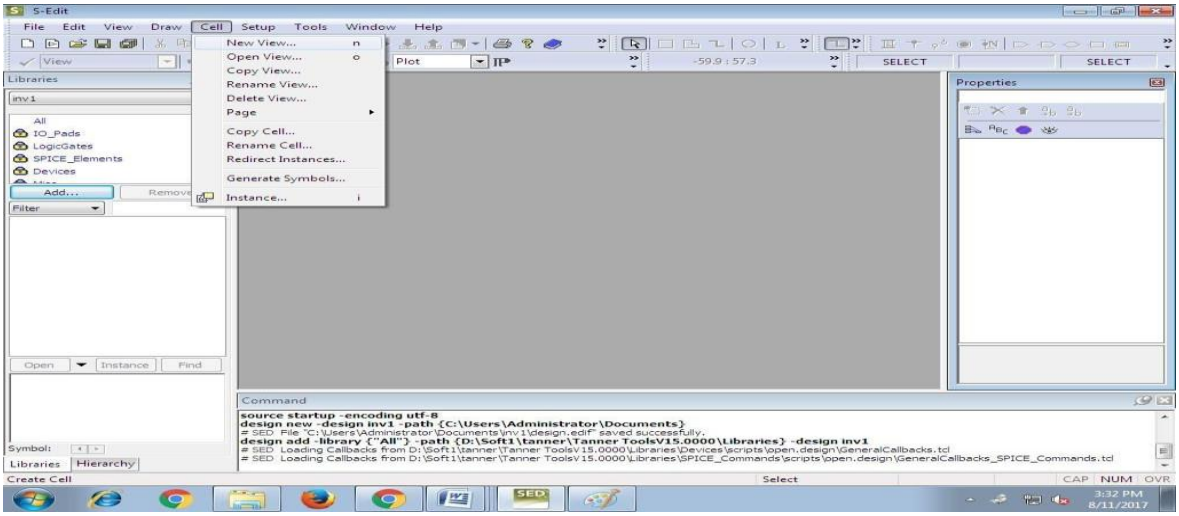


Now to create new cell

Go to cell menu >>

New view -- Select

‘New view’



The new cell will appear like below:

Design = your design name

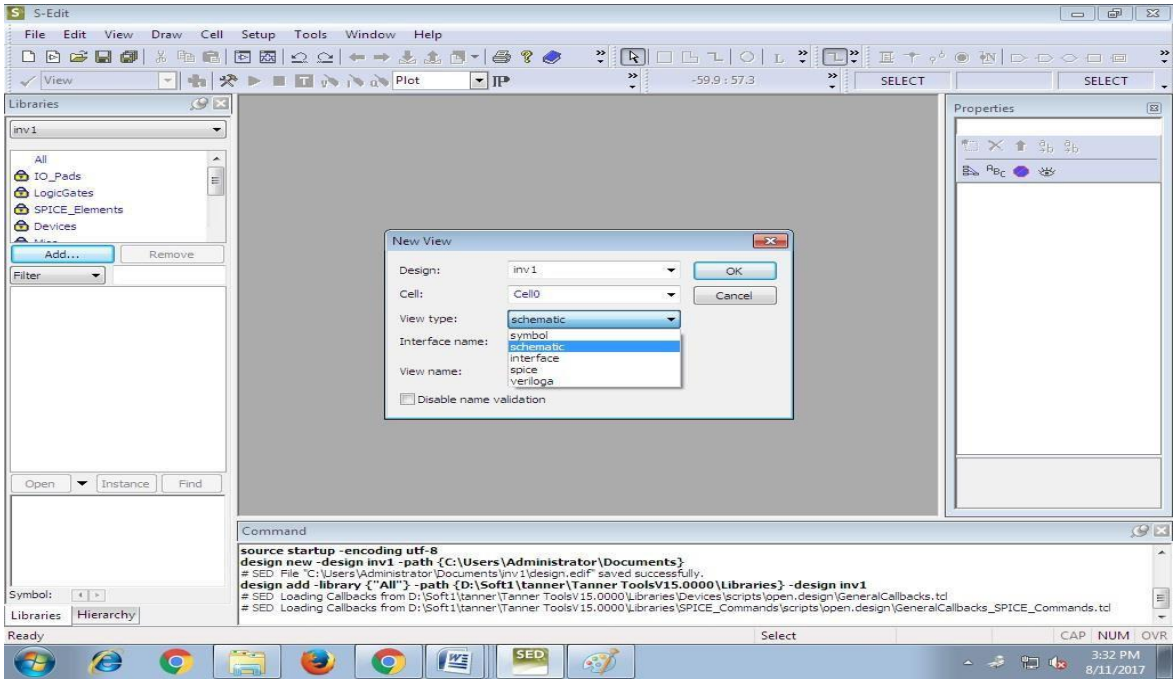
Cell = cell no. (Cell no you can change but your design name inv will be same for different cell. Design name should be changed only when you are going to design another circuit)

View type=schematic

Interface name = “by default”

View name = “by default”

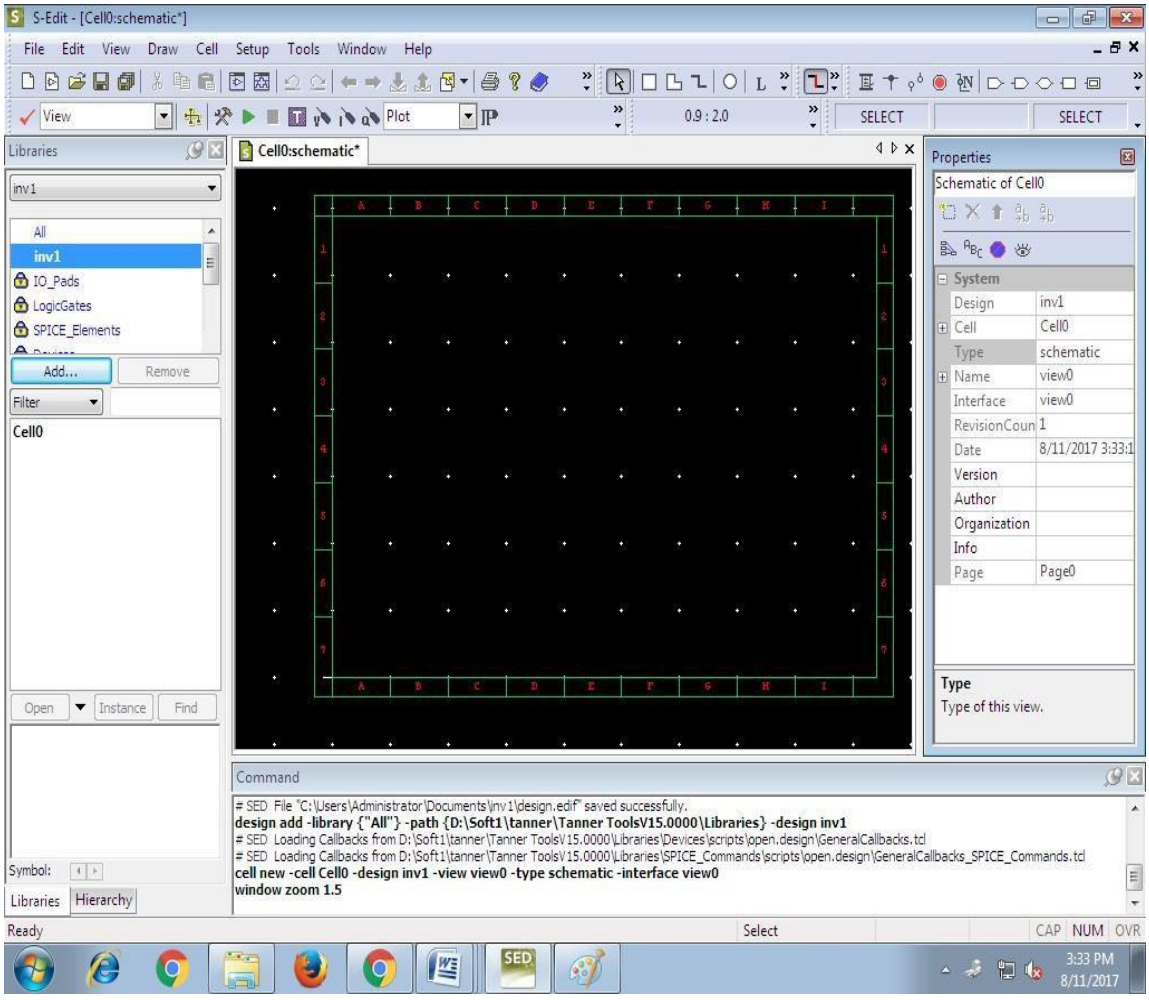
Then press “OK”.



Then a cell will be appeared where we can draw the schematic of any circuit.

In the black window you have seen some white bubble arranged in specific order. This is called grid. You can change grid distance by clicking on black screen and then scroll the mouse.

If you want your screen big enough for design space, then you can close the **Find** & **command window**. You can again bring these windows from **view** menu bar.



To make any circuit schematic:

For example inverter

a) Go to >>libraries & click on device then all devices will be open.

b) Select any device

e.g.:- NMOS Device, then click on, instance (then the dialog box instance cell will appear.)

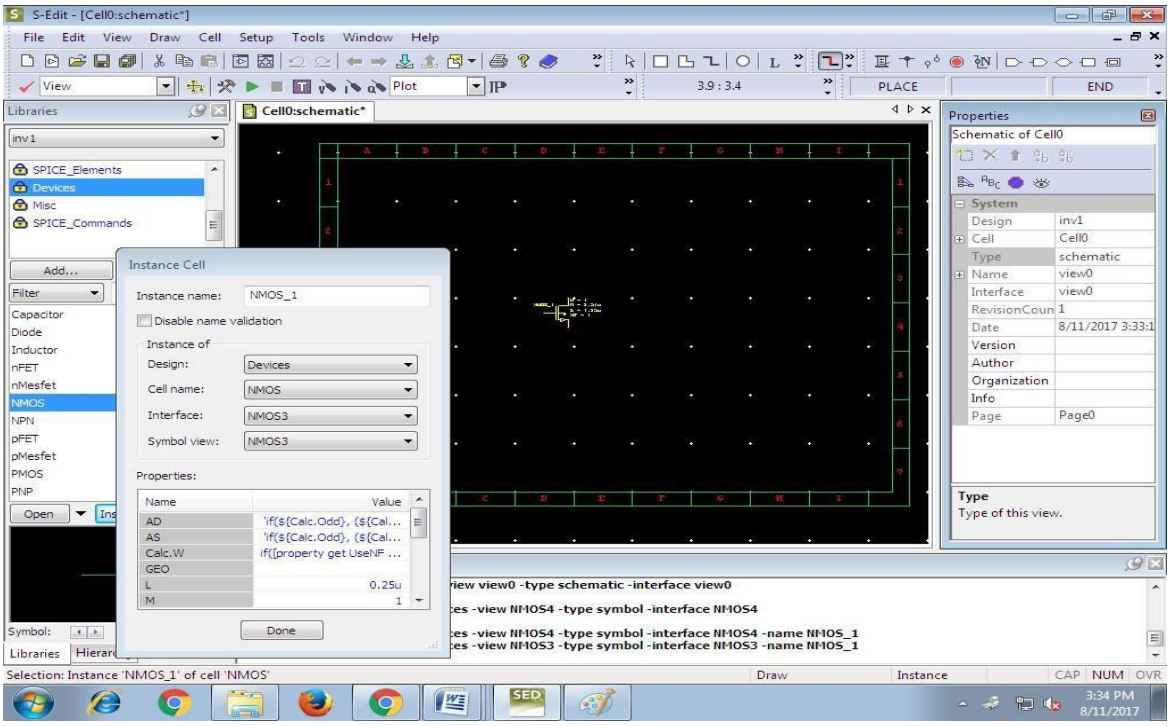
In instance cell

You can change the values of various device parameters according to your requirements.

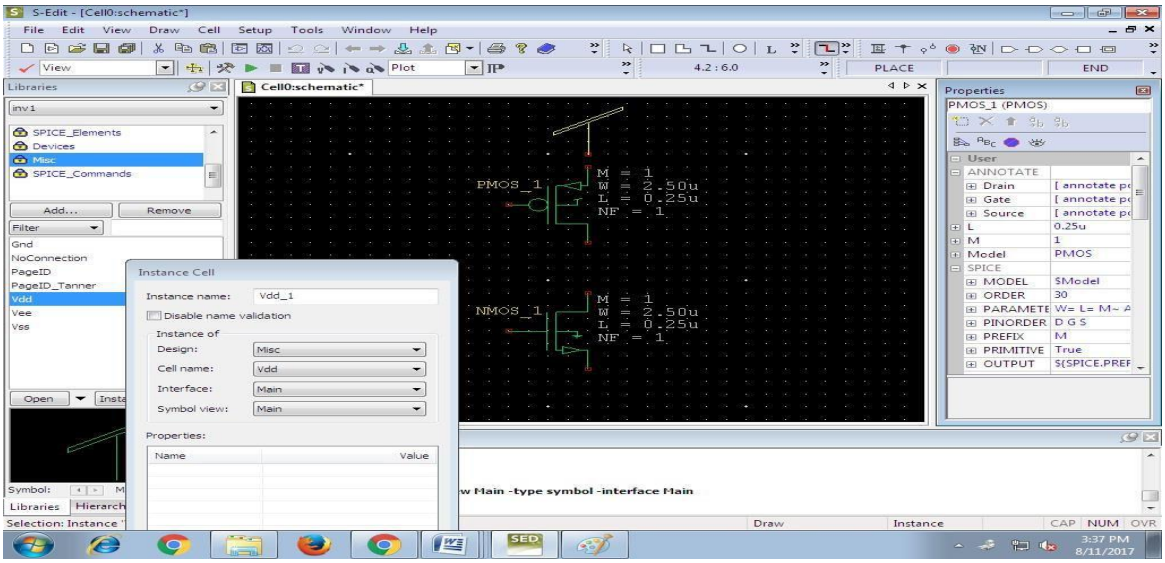
Go to properties >> change the parameter values as your requirement.

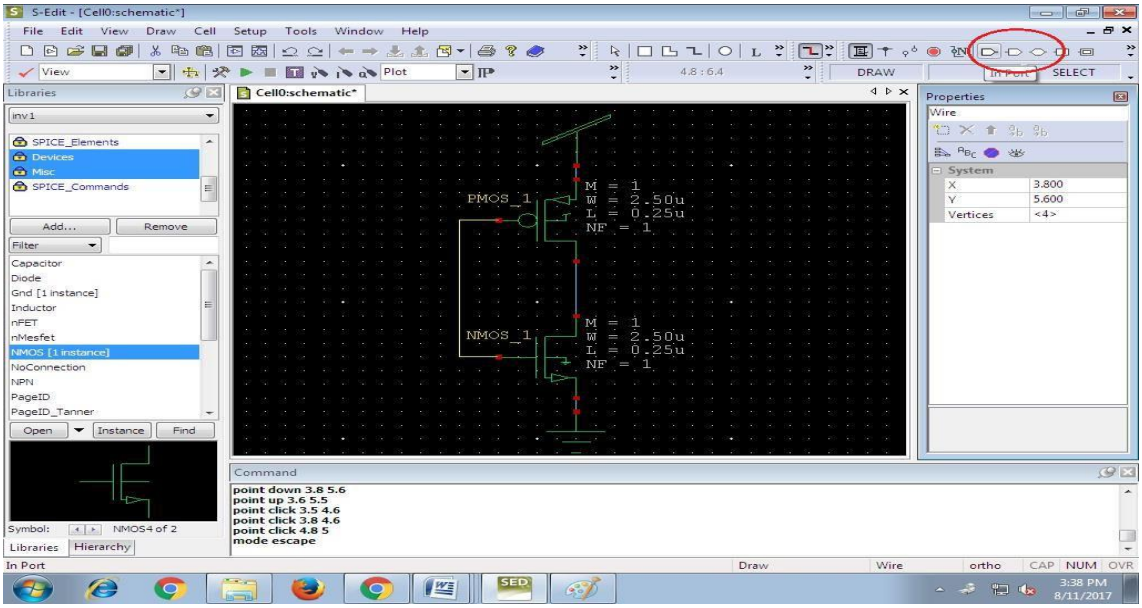
Now before clicking **DONE** you have to DRAG the selected device into the cell and drop it where you want it to FIX.

Then click **DONE** or press **ESC.**

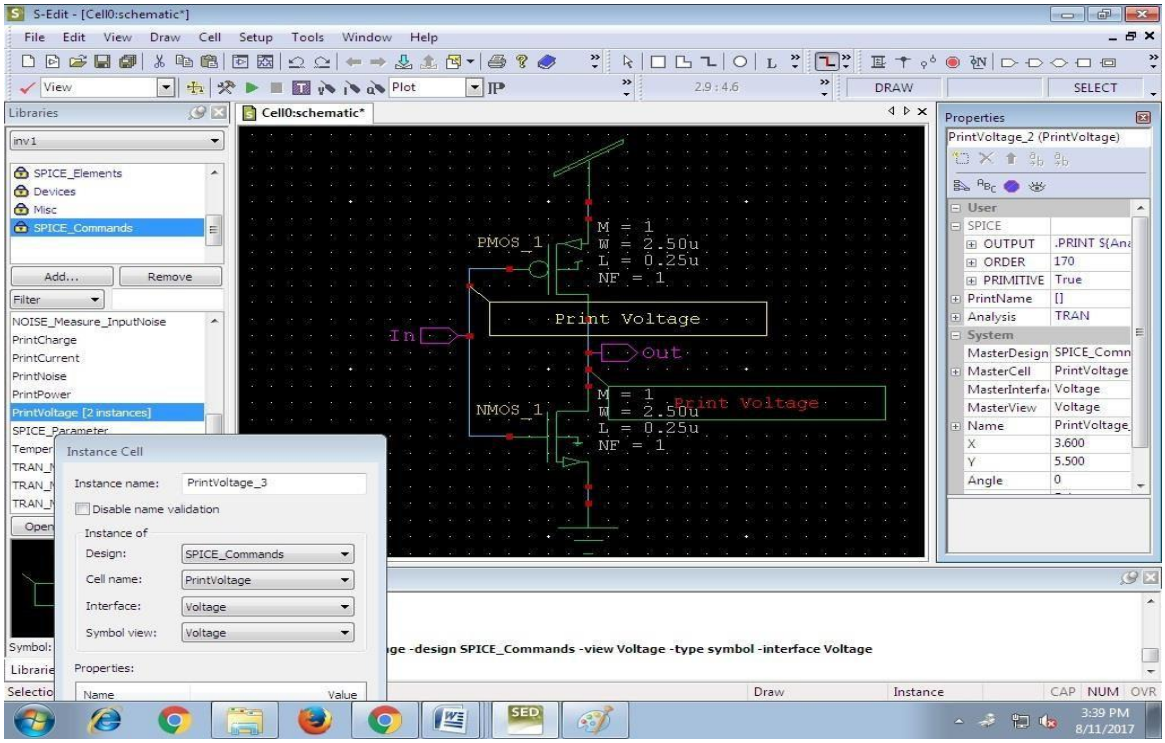


Similarly you can DRAG & DROP any device into the cell for draw your schematic circuit. For inverter we need another PMOS.



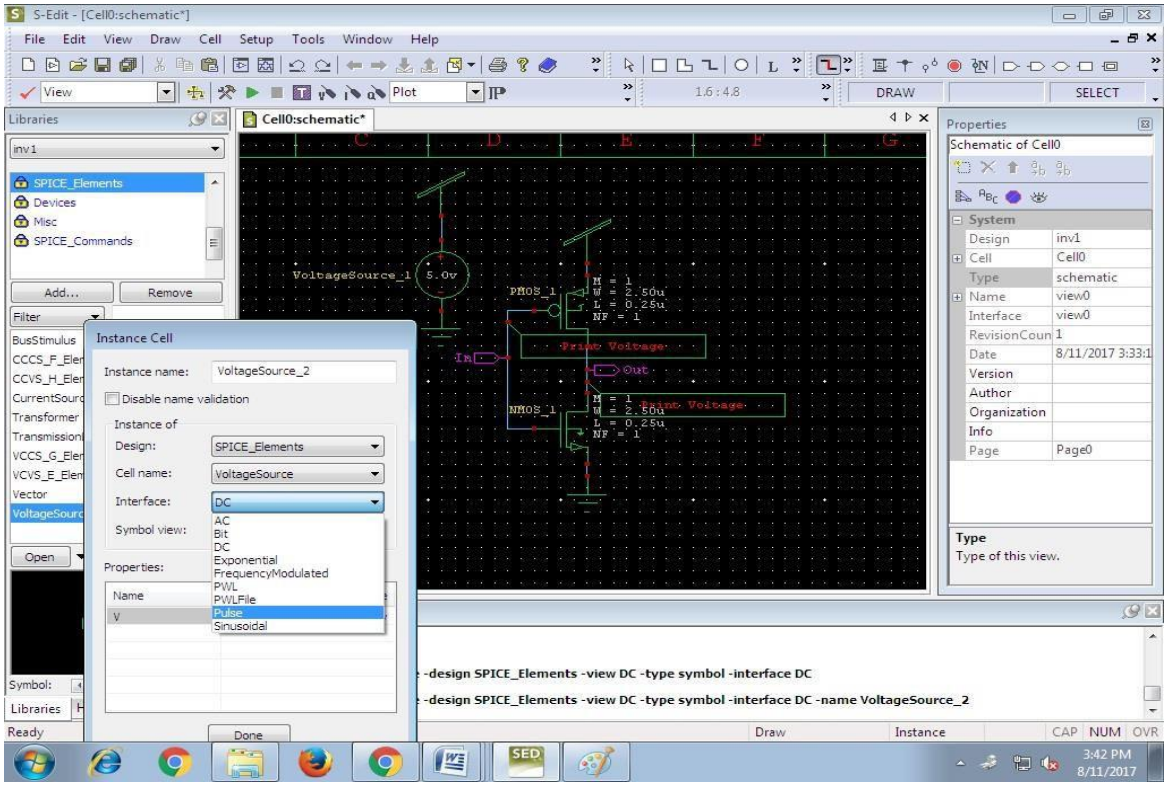


Now add and give Input / Output Port name as you wish in the dialog box.
Then click OK.
NOTE : you can rotate the port (short cut key “R”).

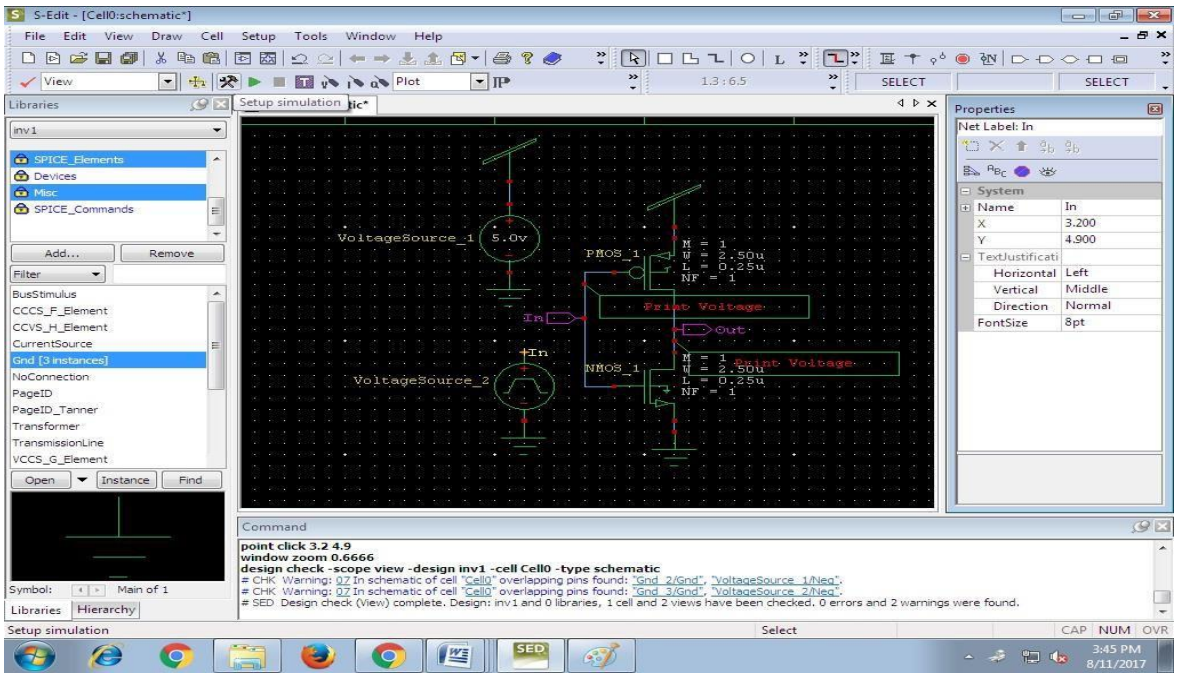


Now, after completed these steps, you should give the supply (VDD) & ground (GND). For that Go to libraries >> MISC >>Select VDD or GND

Now you have to create a source of VDD. For that go to libraries >>spice element >> and then select voltage source of type DC . you can give any value in vdd .let’s take vdd =5v.

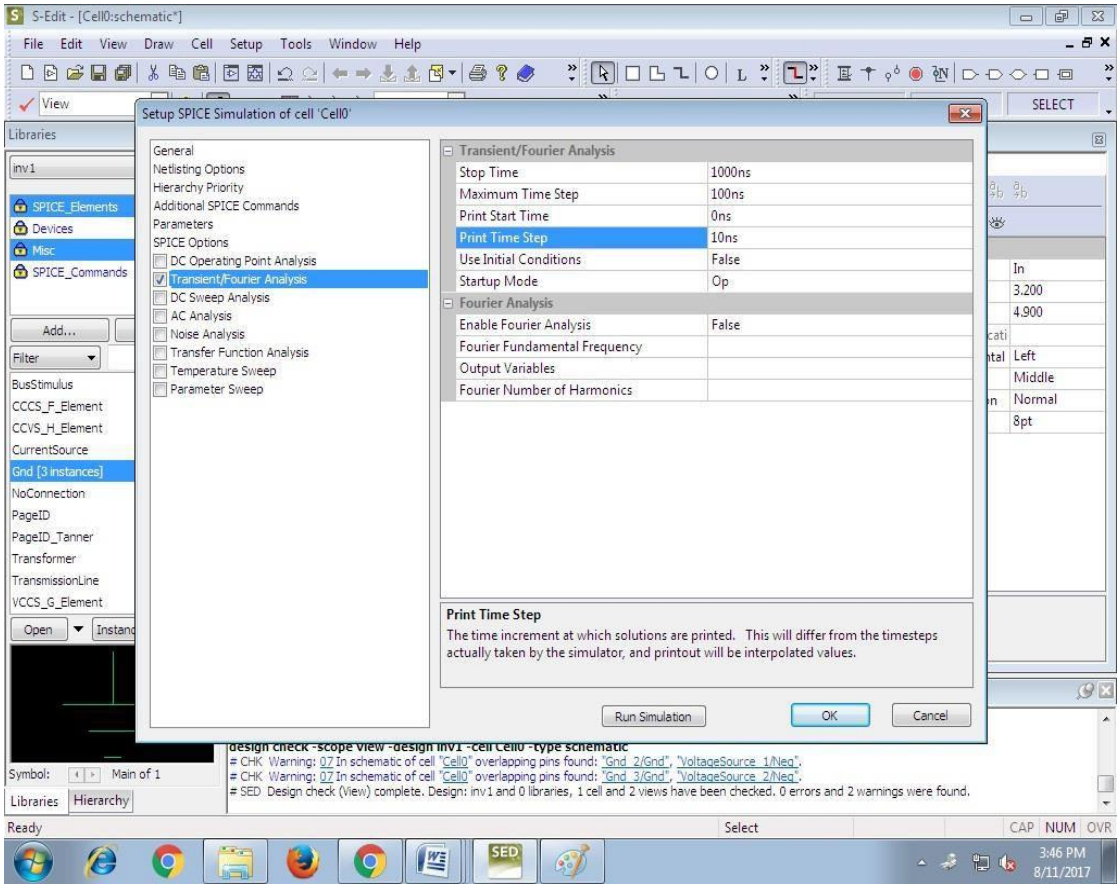


The complete circuit Diagram of the design (Inverter). By doing all the above steps you have completed schematic of Inverter

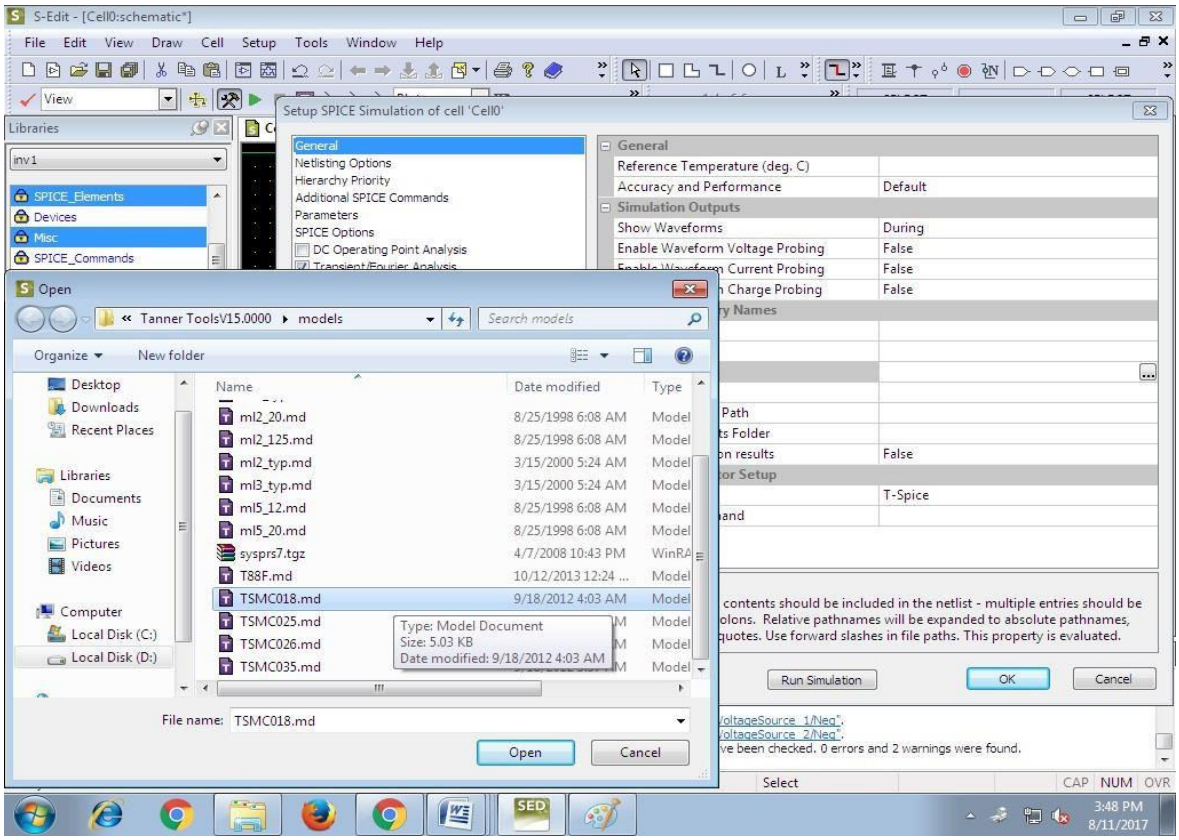


After verifying the design, do simulation by doing following

Settings: Go to setup spice->Transient Fourier Analysis

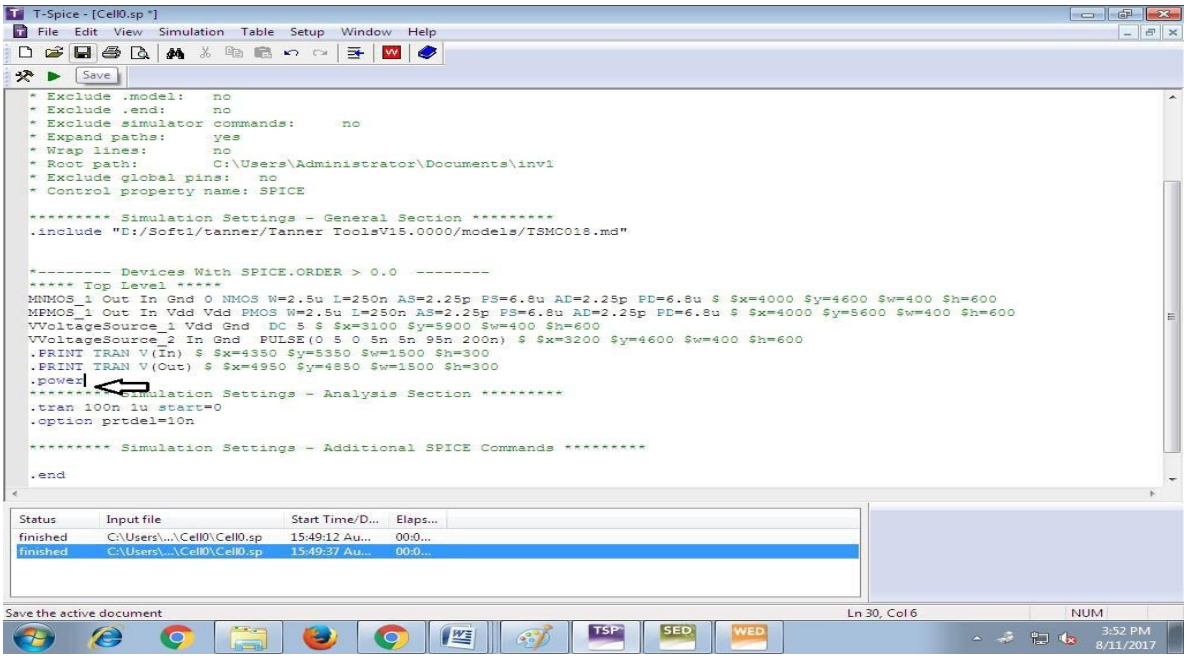


Include setup spice->General -> Include files -> model TSMC018 ->ok



Run simulation to get the waveforms.

For power calculation press T-spice button (beside simulation button), write ".power" in t-spice window. Save the changes and run the T-spice file.



CHAPTER 4

EXISTING AND PROPOSED ARCHITECTURE

4.1 BASIC LOGIC GATES

4.1.1 LOGIC EQUATION FOR XNOR GATE

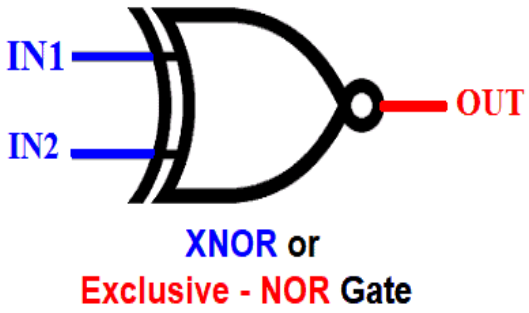
The XNOR gate functions are shown in Table 4.1 and denoted by this "⊙" .

B	A	XNOR
0	0	1
0	1	0
1	0	0
1	1	1

Table 4.1. XNOR Gate Function

Functionality: The XNOR gate is the logical opposite of the XOR (Exclusive OR) gate.

Symbol:



The XNOR gate is often represented by an XOR gate symbol with a circle (inversion bubble) at the output.

Boolean Expression:

The XNOR operation can be expressed as Y = A ⊙ B.

Where,

A and B are the inputs,

and Y is the output.

4.1.2 LOGIC EQUATION FOR XOR GATE

In XOR gate, or Exclusive OR gate, is a logic gate that outputs a "1" (true) only when the inputs are different, and a "0" (false) when the inputs are the same, often denoted by the symbol "⊕" or "⊻" in Boolean algebra.

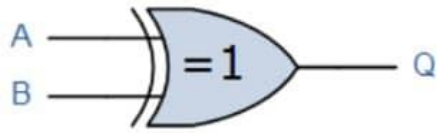
Symbol	Truth Table		
 2-input Ex-OR Gate	A	B	Q
	0	0	0
	0	1	1
	1	0	1
	1	1	0
Boolean Expression Q = A XOR B			

TABLE 4.2 : TRUTH TABLE OF XOR GATE

Function:

The XOR gate performs the exclusive disjunction operation, meaning it outputs "1" if and only if one of the inputs is "1" and the other is "0".

Symbol:

The most common symbol for an XOR gate is a plus sign (+) enclosed in a circle (⊕). In some cases, the DIN symbol ⊻ is used. In C-like languages, the caret symbol (^) is used to denote bitwise XOR.

Boolean Expression:

The Boolean expression for an XOR gate is: Y = A ⊕ B.

Where,

A and B are inputs,

and output Y .

4.1.3 LOGIC EQUATIONS FOR THE PROPOSED FULL ADDERS

The logical function of the 1 bit full adder operation equations presented below can be stated as follows: given the inputs *A*, *B* and *Cin* which calculate two 1-bit outputs *Sum*, for sum and *Cout*, for carry out.

$$\mathbf{S = A \oplus B \oplus Cin}$$

$$\mathbf{Cout = (A \cdot B) + (Cin \cdot (A \oplus B)).}$$

Jyh-Ming Wang at el to design 4 transistor XNOR gate as shown in fig.4.1. This design no longer need complementary signal inputs and only one poor signal level on output end. Author define the defect property of a 4-transistor type is that the output level will be higher or lower than the normal case by the voltage |Vth|, the threshold voltage of MOS. Under the condition of |Vth| value, this poor level can still drive the inverter and make the inverter action correct.

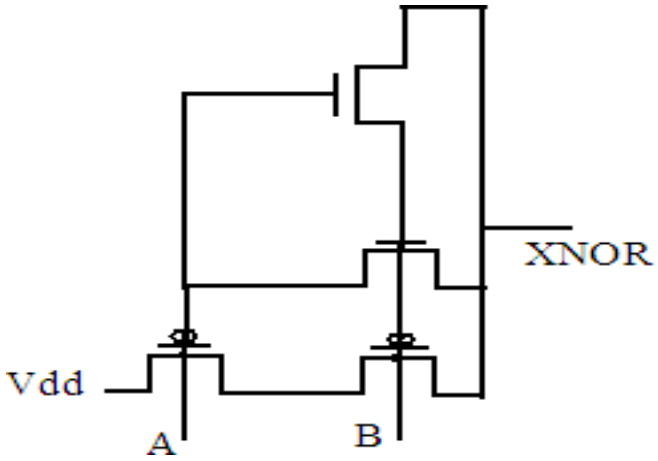


Figure.4.1:-4T XNOR Gate

Hung Tien Bui at el to design 4 transistor XNOR gate as shown in fig. 4.2 that is named Groundless, because there is no ground and show the better performance previous design XNOR gate.

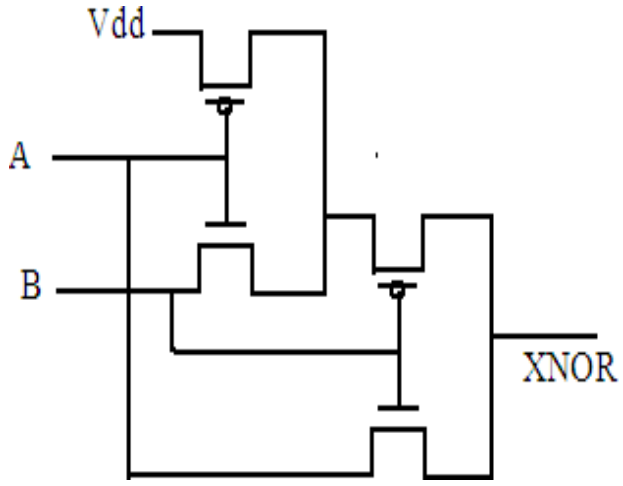


Figure 4.2-4T XNOR Gate

J. Wang at el to design 4 transistor XNOR gate as shown in fig 4.4. It is inverter base XNOR gate.

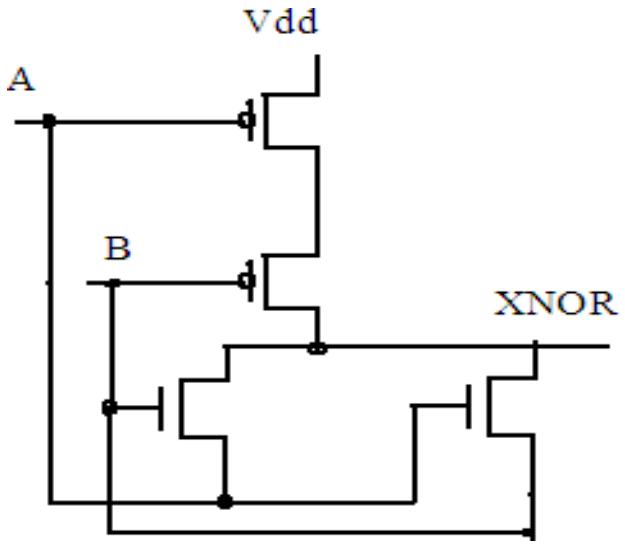


Fig 4.3 4T XNOR Gate

Sreehari Veeramachaneni at el to design XNOR gates using 3 transistors (3-T) shown in fig 4.4. transistors has a small delay of mere 1 transistor (1-T). However, for certain input combinations, they give bad output logic levels.

Author manipulates the (*W/L*) ratios of PMOS and NMOS transistors to solve this problem until an acceptable logic level is restored. The image depicts a 3T XNOR gate circuit diagram. This circuit uses three transistors to implement the XNOR logic function. The XNOR gate, also known as exclusive NOR gate, produces a high output (1) only when both of its inputs are the same (either both 0 or both 1).

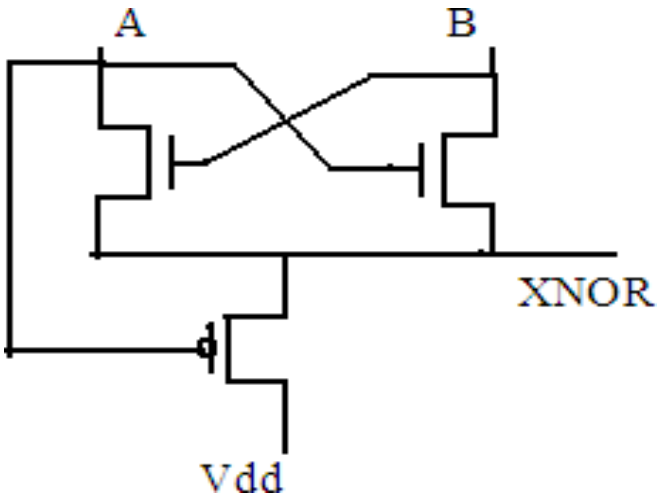


Figure 4.4: 3T XNOR Gate

4.2 EXISTING METHODOLY

Full Adder in 8T logic embodies only 8 transistors and the number of interconnections between them is highly reduced. Having each transistor a lower interconnection capacitance, the W/L can be close to the minimum value and the power consumption is decreased. The total input capacitance consists of the input node (in) and interconnection capacitance obtained by post-layout parasitic extraction, is 2 fF..

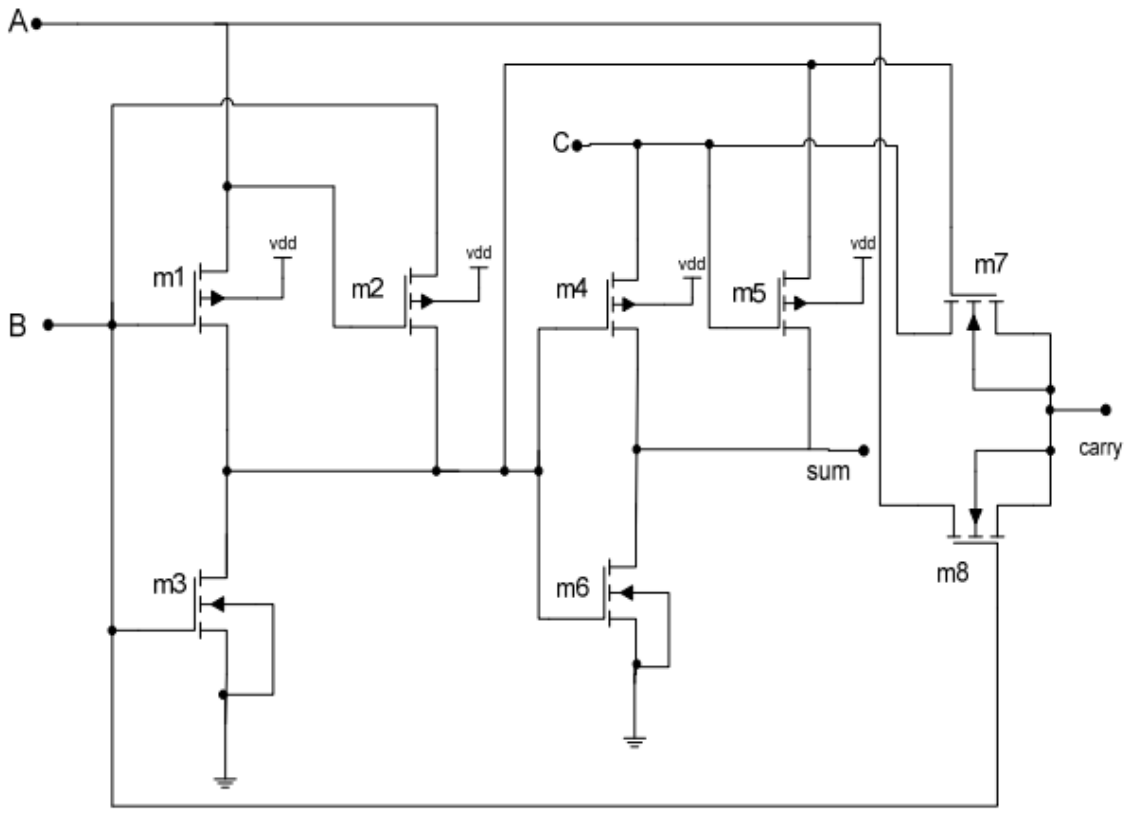


Figure 4.5 The full adder cell with 8T Structure

The Full Adder operates in 100MHz range. Infact, in addition to normal transistors, circuits are tested in corner cases with fast and slow transistors and their combination, too. In each stage one of the components FF, SS, FS, SF are replaced instead of normal transistors in circuit and are perused circuit functions. The difference in this stage is in consumption power and falling and rising times so this subject looks simple due to the difference in nMOS and pMOS transistors speed.

4.3 DISADVANTAGES OF EXISTING METHOD

The existing methods for full adder designs, particularly those based on traditional CMOS logic, have several significant disadvantages. First, they typically suffer from higher power consumption due to dynamic power dissipation and leakage currents, making them unsuitable for low-power applications, especially in battery-operated devices. Conventional full adders, often using 4T or 6T CMOS gates, also require a larger area because of the higher transistor count, which leads to inefficiencies in high-density integrated circuits. This increased area not only raises the cost of fabrication but also makes these designs less practical for compact, high-performance systems.

Additionally, traditional designs tend to have longer propagation delays, which slow down the overall speed of the circuit, limiting their performance in high-speed applications like processors and arithmetic logic units. These methods also fail to achieve an optimal power-speed trade-off, as they prioritize functionality and speed over energy efficiency, which can be a significant drawback in low-power or mobile devices.

Furthermore, conventional full adders are prone to higher leakage currents, particularly at smaller technology nodes, contributing to static power dissipation. Finally, traditional designs often do not perform well at low voltages, making them inefficient for applications that require low-power operation, such as IoT devices.

In contrast, the proposed 6T full adder with 2T XOR-XNOR logic addresses these limitations by reducing transistor count, minimizing power consumption, and improving overall efficiency, making it better suited for modern low-power VLSI systems they typically suffer from higher power consumption due to dynamic power dissipation and leakage currents, making them unsuitable for low-power applications, especially in battery-operated devices. Conventional full adders, often using 4T or 6T CMOS gates, also require a larger area because of the higher transistor count, which leads to inefficiencies in high-density integrated circuits. This increased area not only raises the cost of fabrication but also makes these designs less practical for compact, high-performance systems.

4.4 PROPOSED ARCHITECTURE

4.4.1 2T XNOR GATE

On the 2-transistor design, the new proposed structures require non-complementary inputs and their output will be nearly perfect. The configurations are shown in Fig. 4.6. For the XNOR function, the output signal in the case of AB = 00,01, 11 will be complete. While AB = 10, NMOS will be on and pass the poor ―HI‖ signal level to the output end.The input combinations, they give bad output logic levels but we manipulate the (*W/L*) ratios of PMOS and NMOS transistors to solve this problem until an acceptable logic level is restored.

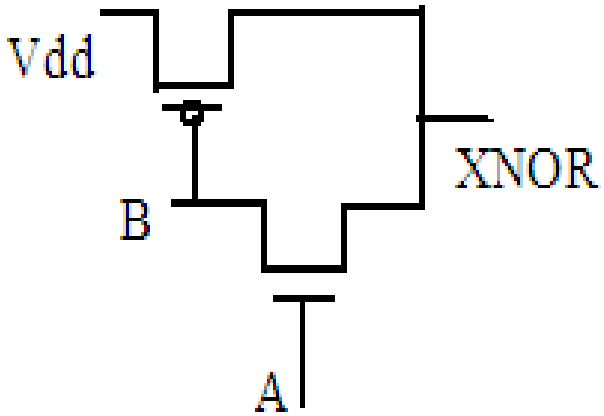


Figure.4.6 -Proposed 2T XNOR Gate

4.4.2 THE NEW DIRECT DESIGN FOR THREE-INPUT XNOR FUNCTION

The three-input XNOR function is usually implemented by cascading two two-input XNOR gates. Hence, the performance of the two-input XNOR gate affects inherently the performance of the assembled three inputs XNOR function very much.

Design a new structure of three-input function on the transistor level as shown in fig.4.7. The basic structure of the proposed three-input XNOR function utilizes the least number of transistors and no complementary input signals are needed.

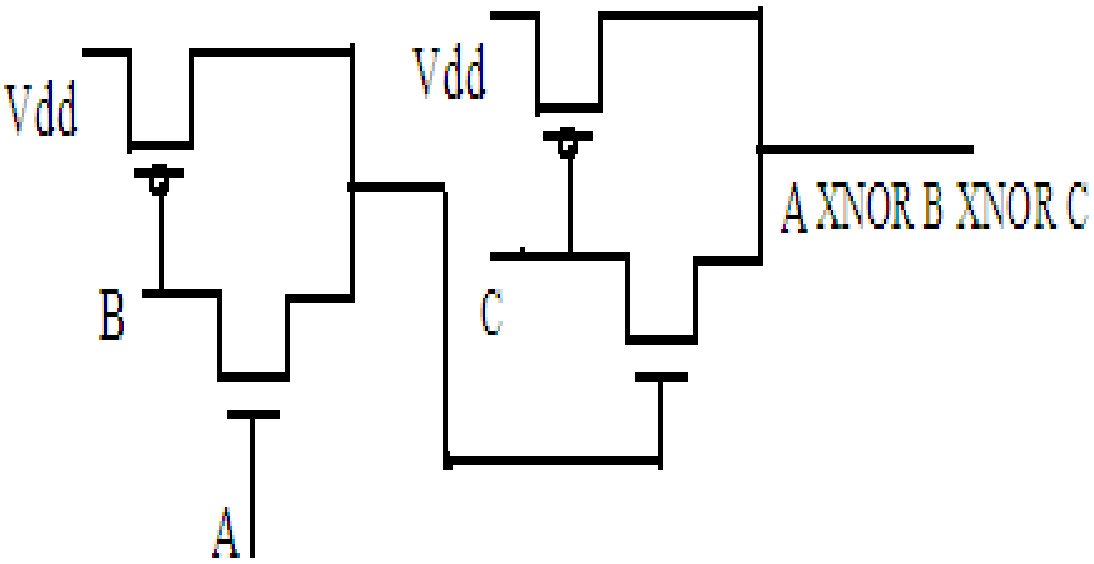


Figure.4.7. A new cascaded design of three-input XNOR function.

4.4.3. FULL ADDER

The full adder is used to add three 1-bit binary numbers A, B, and carry C. The full adder has three input states and two output states i.e., sum and carry.

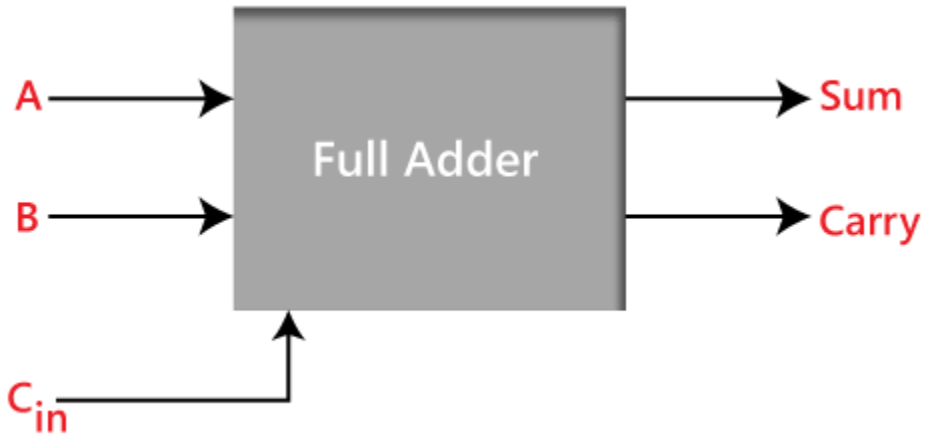


FIGURE 4.8. BLOCK DIAGRAM OF FULL ADDER

In the above FIG,

1. 'A' and' B' are the input variables. These variables represent the two significant bits which are going to be added

2. 'C_{in}' is the third input which represents the carry. From the previous lower significant position, the carry bit is fetched.

3. The 'Sum' and 'Carry' are the output variables that define the output values.

4. The eight rows under the input variable designate all possible combinations of 0 and 1 that can occur in these variables.

A	B	C	SUM(OUTPUT)	CARRY(OUTPUT)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

TABLE 4.3- TRUTH TABLE OF FULL ADDER

Sum:

Perform the XOR operation of input A and B.

Perform the XOR operation of the outcome with carry. So, the sum is (A XOR B) XOR C_{in} which is also represented as:

$(A \oplus B) \oplus C_{in.}$

Carry:

Perform the 'AND' operation of input A and B.

Perform the 'XOR' operation of input A and B.

Perform the 'OR' operations of both the outputs that come from the previous two steps.

So the 'Carry' can be represented as:

$$(A \oplus B) \oplus C_{in}$$

4.4.4 THE PROPOSED FULL ADDERS USING 2T XNOR GATE

As shown in Fig. .6-T full adder contains three modules—two 3-T XNOR gates and a 2-transistor multiplexer (2-T MUX) as shown in Fig. 4.9.

The Sum and Cout can be obtained using (1) and (2) respectively. Owing to the appealing traits of a small number of transistors and a mere 2-transistor (2-T) delay, it can work at high speed with low power dissipation.

The sum output is basically obtained by a cascaded XNORing of the three inputs in accordance with equation 2. The carry output is obtained in accordance with equation . The final sum of the products is obtained using a wired XNOR logic. The W/L ratios of transistors M1-M3 are 70/.18 µm .The W/L ratios of transistors M2 and M4 are same taken as 2/.90µm.

The W/L ratios of transistors M5 is taken as 4/.18 µm and M4.4. is taken as 0.1/0.18 µm It is quite evident from figure 4.3 that two stage delays are required to obtain the sum output and at most two stage delays are required to obtain. We design a new structure of three-input function on the transistor level as shown in fig.4.9. The basic structure of the proposed three-input XNOR function utilizes the least number of transistors and no complementary input signals are needed.

The 6T Full adder was consists of three modules, two 2-T XNOR gates, and a 2-T multiplexer. The corresponding equations can be used to determine the Sum and C-out. It may operate at fast speed with minimal power dissipation due to the appealing characteristics of a limited number of transistors and a modest 2-T delay. Basically, the three inputs are cascaded XNOR to produce the sum output in line with equation. Equation is followed to acquire the carry output. Through the use of wired XNOR logic, the final sum of the products is determined.

The Logical equations for the 6T Full adder using XNOR,

$$\text{Sum} => (A \text{ XNOR } B) \text{ XNOR } C$$

$$\text{Carry} => AB + BC + CA$$

$$= (A \text{ XNOR } B)\, A + (A \text{ XNOR } B)' \, C.$$

Figure 4.9 represents the Schematic of the 6T Full adder designed using 2T XNOR..

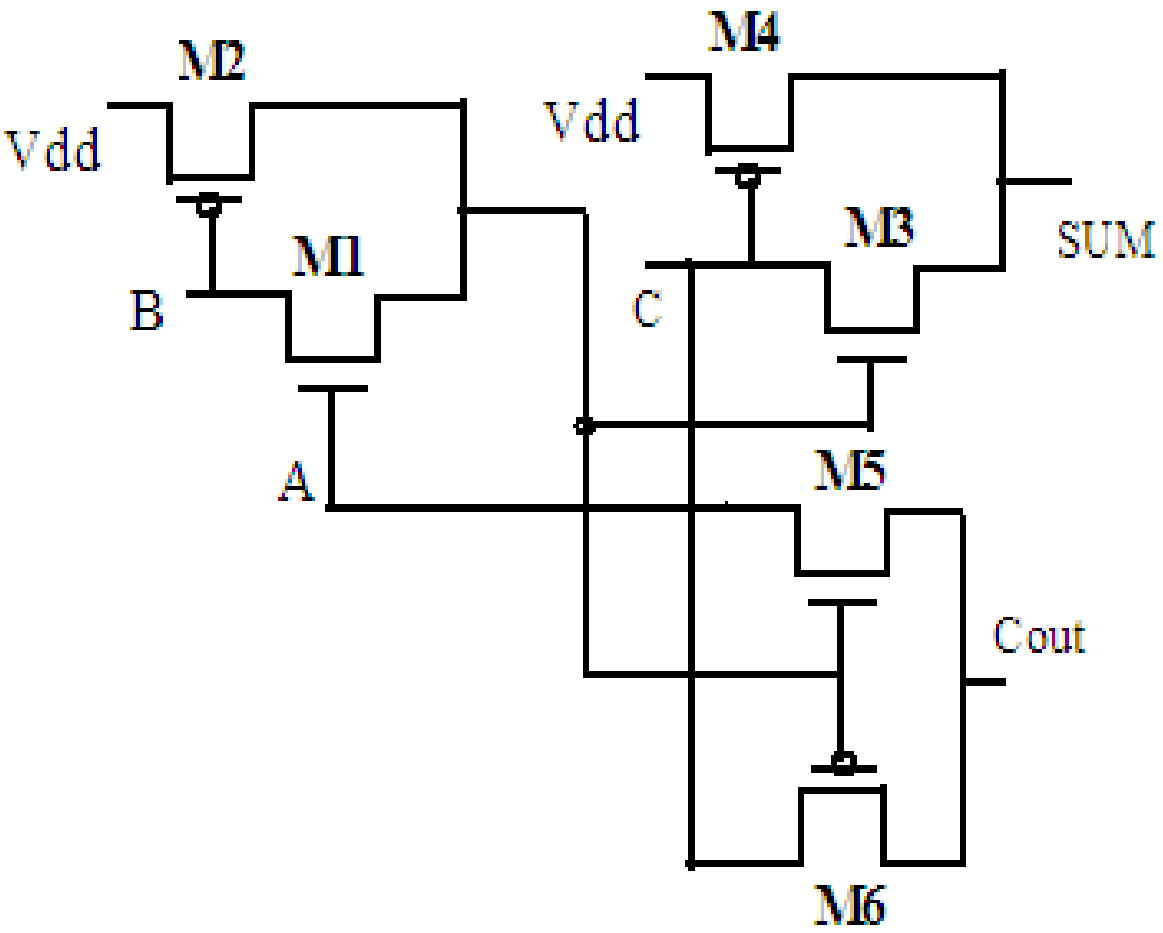


Figure 4.9 6T full adder Using XNOR Logic

The figure 4.10 shows a schematic diagram of a full adder circuit. The circuit takes two inputs, A and B, and a carry-in input, Cin, and produces two outputs: Sum and Carry. The circuit consists of several NMOS and PMOS transistors connected in a specific configuration to perform the addition operation. The labels in the image provide information about the components and their properties, such as transistor sizes and voltage levels.

The schematic represents a full-adder circuit designed using MOSFET transistors. It takes three input signals—A, B, and C (carry-in)—and processes them through a series of transistor-based logic gates to produce two outputs: Sum and Carry. The circuit operates with a 5V power source and includes clocked voltage sources for testing purposes. The interconnected transistors form the essential XOR, AND, and OR gates needed for addition operations. By analyzing the signal flow, one can observe how binary addition is implemented at the hardware level, demonstrating fundamental digital logic design principles.

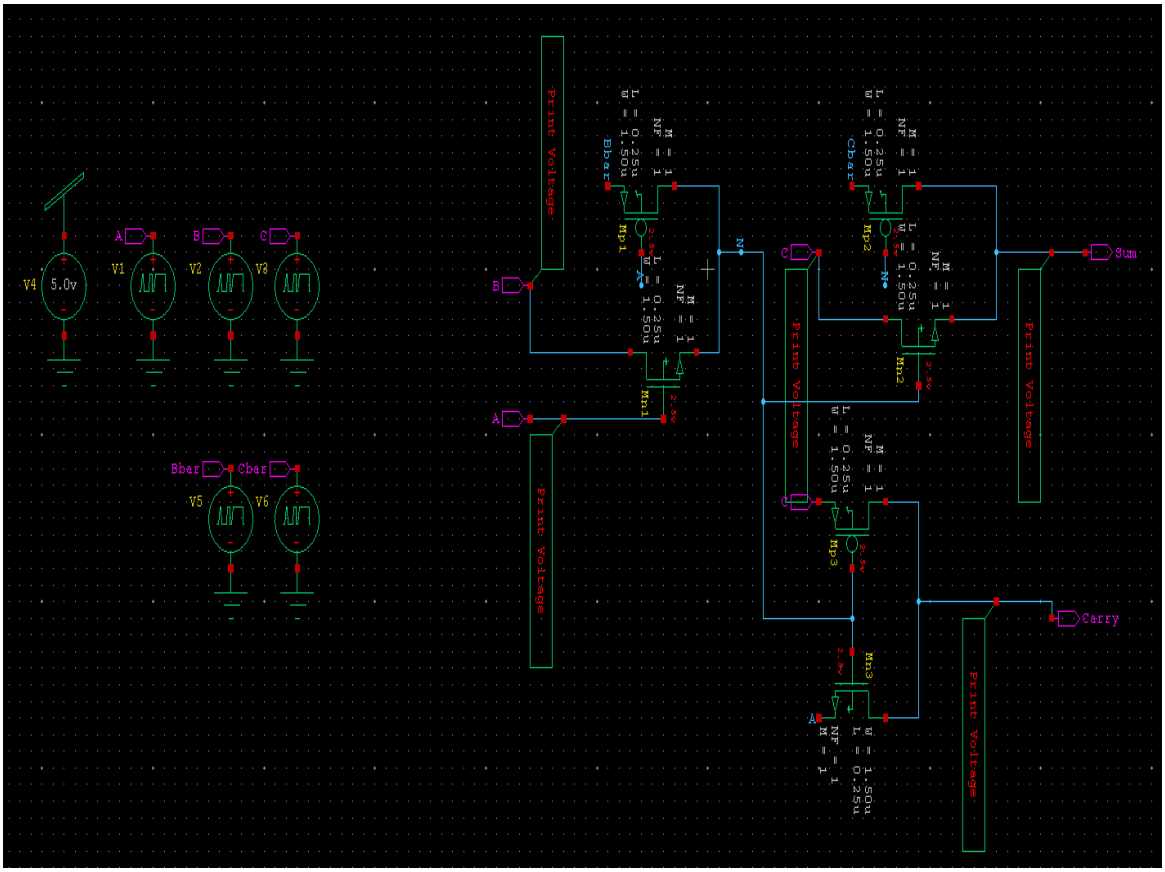


Figure 4.10 Schematic 6T full adder Using XNOR Logic

4.4.5 THE PROPOSED FULL ADDERS USING 2T XOR GATE

A 6T Full adder was proposed utilizing a 2T XNOR gate and PTL with TSPICE [2]. Proposed design uses Cadence Virtuoso 90nm technology during design, which significantly reduces the PDP of this circuit.

The structure on the 2-transistor design needs noncomplementary inputs, and their output will be almost flawless. The configurations for the XNOR function are illustrated, the output signal will be strong if AB = 00, 01, or 11. NMOS will turn on while AB = 10 and send the weak "HI" signal level as a response. Typically, two two-input XNOR gates are cascaded to create the three-input XNOR function.

Therefore, the performance of the built three input XNOR function is greatly influenced by the performance of the two-input XNOR gate . influenced by the performance of the two-input XNOR gate. The 6T full adder sum proposed is produced using a 2T XOR Module Twice, and the carry is produced using NMOS and PMOS Pass Transistor Logic.

This design uses (A XOR B) signal to select one out of two options before passing it to a pass transistor multiplexer comprised of two transistors.

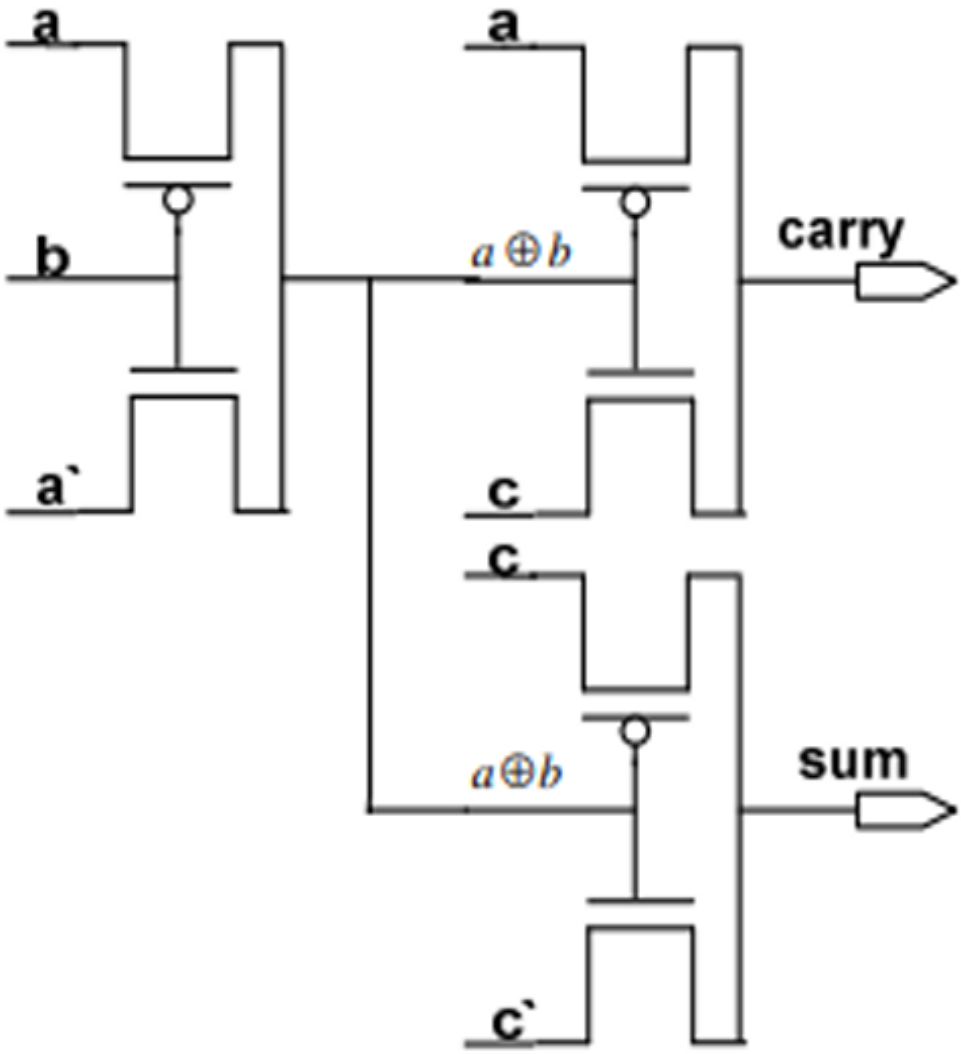


Figure 4.11 - 6T Full Adder using 2T XOR Logic

The multiplexer receives two commands: one to generate carry (A XOR B) to select between a, c, and the other to generate sum (A XOR B) to select between c', c.

The Logical equations for the 6T Full adder using XOR,

$$\text{Sum} => (A \oplus B) \oplus C => (A \oplus B)\, C' + (A \oplus B)'C$$

$$\text{Carry} => AB + BC + CA = (A \oplus B)'A + (A \oplus B)\, C$$

Figure 4.12 represents the Schematic of the 6T Full adder designed using 2T XOR Logic.

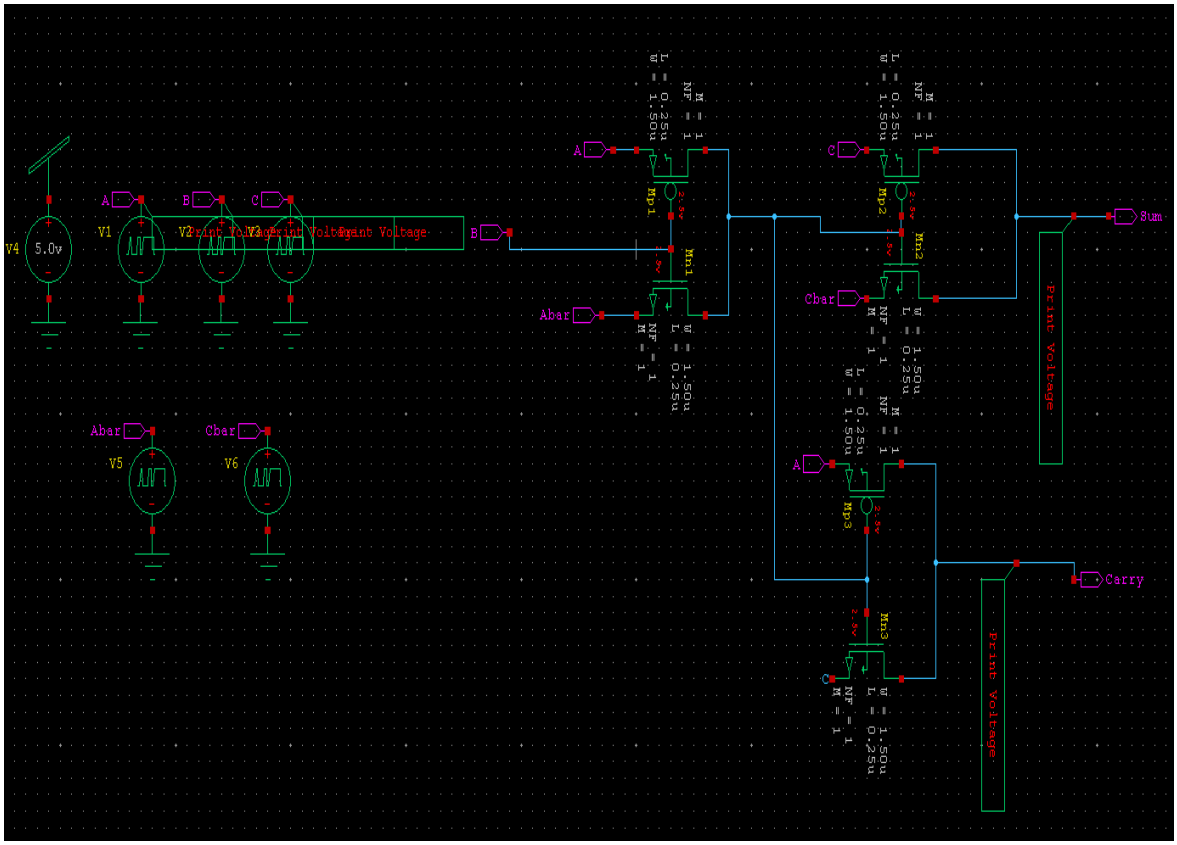


Figure 4.12 Schematic 6T Full Adder using 2T XOR Logic

The fig shows a transistor-level schematic of a full-adder circuit, a fundamental digital logic component used for binary addition. The circuit consists of MOSFET transistors arranged to implement XOR, AND, and OR logic gates, which are essential for computing the sum and carry outputs. The inputs, labeled as A, B, and C, represent the binary digits to be added, while the outputs Sum and Carry indicate the result of the addition.

On the left side of the schematic, voltage sources provide the necessary power and clock signals, ensuring proper operation. Additional labeled nodes, such as Abar and Cbar, represent the complemented (inverted) signals used in logic processing. The transistors are strategically connected to form logic gates, with wires clearly illustrating the flow of signals. The "Print Voltage" labels at various points indicate test points where voltages can be monitored to verify circuit functionality.

This schematic is particularly useful for understanding the transistor-level implementation of arithmetic circuits in digital systems. It demonstrates how simple switches (MOSFETs) can be combined to execute complex logical operations, forming the basis of processors and computational hardware.

CHAPTER 5
SIMULATION RESULTS AND PERFORMANCE EVALUATION METRICS

5.1 SIMULATION RESULTS OF 6T FULL ADDER USING XNOR GATE

The proposed 2T XNOR gates, three previous 4T, 3T XNOR gate, three input XNOR gate and 1-bit full adders are simulated using T-spice in Tanner Tools. All the results are obtained in 180nm CMOS process technology with a 5V supply voltage. In order to establish an impartial simulation circumstance, authors prefer the input patterns ,which covers every possible inputs combination of A, B, and Cin.

The delay has been measure between the time when the changing input reaches 50% of voltage level to the time it output reaches 50% of voltage level for both rising and fall transition for Sum and Cout. The power delay product (PDP) is measured as the product of the average delay and the average power. The output waveform of the proposed circuit is shown in fig 4.10.

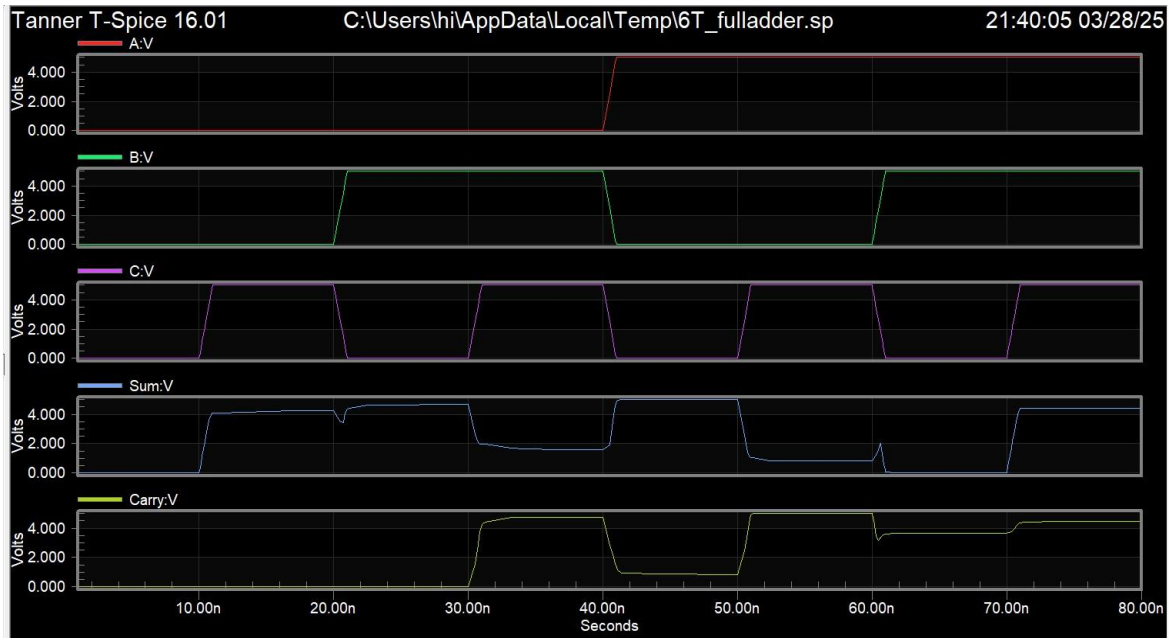


FIGURE 5.1 OUTPUT WAVEFORM OF 6T FULL ADDER USING XNOR LOGIC

5.2 SIMULATION RESULTS OF 6T FULL ADDER USING XOR GATE

The proposed 2T XOR gates, three previous 4T, 3T XOR gate, three input XOR gate and 1-bit full adders are simulated using T-spice in Tanner Tools. All the results are obtained in 180nm CMOS process technology with a 5V supply voltage. In order to establish an

impartial simulation circumstance, authors prefer the input patterns ,which covers every possible inputs combination of A, B, and Cin.

The delay has been measure between the time when the changing input reaches 50% of voltage level to the time it output reaches 50% of voltage level for both rising and fall transition for Sum and Cout. The power delay product (PDP) is measured as the product of the average delay and the average power. The output waveform of the proposed circuit is shown in fig 4.12.

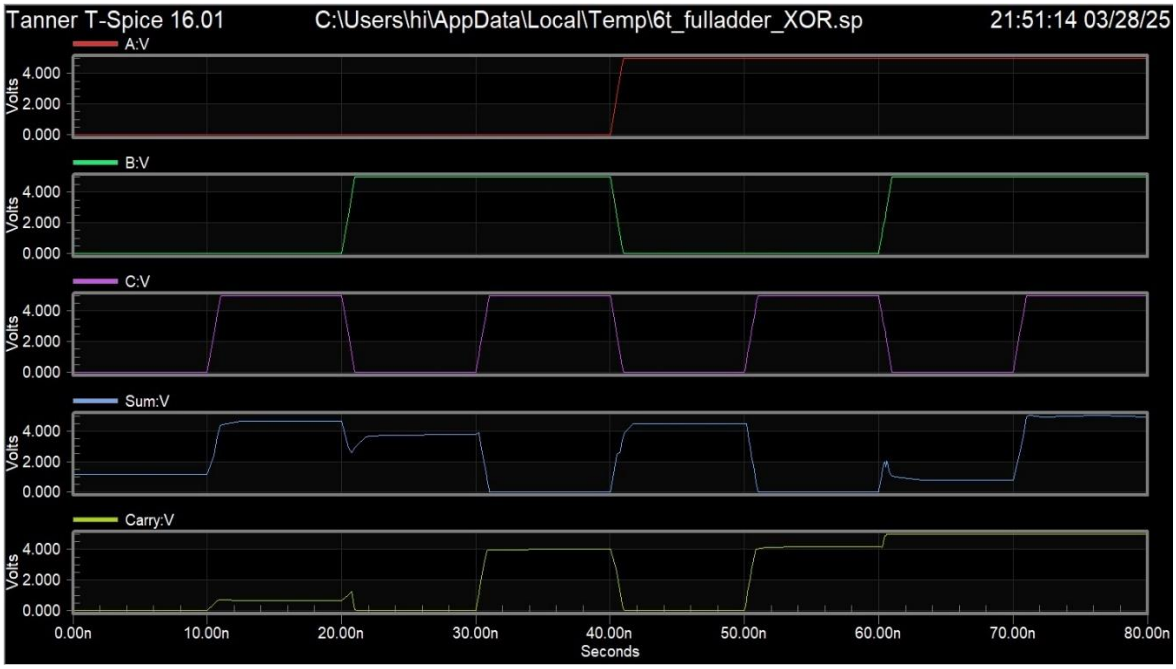


FIGURE 5.2 OUTPUT WAVEFORM OF 6T FULL ADDER USING XOR LOGIC

5.3 PERFORMANCE EVALUATION METRICS

5.3.1 PERFORMANCE EVALUATION METRICS OF 6T FULL ADDER USING XNOR LOGIC

The simulation report details the configuration and performance of an electronic circuit analysis, listing six MOSFETs, voltage sources, and various nodes. The power results indicate an average power consumption of approximately 0.229 mW, with a peak of 1.77 mW at 31 ns and a minimum of 1.07 nW at 100 ns. The computational breakdown shows parsing took 0.09 seconds, setup 0.03 seconds, DC operating point 0.01 seconds, transient analysis 0.04 seconds, and overhead 1.14 seconds, totaling 1.31 seconds for completion. The simulation was successfully executed.

```
General options:
        threads = 1

 Device and node counts:
              MOSFETs -       6
    MOSFET geometries -       2
      Voltage sources -       6
          Subcircuits -       0
    Model Definitions -       6
      Computed Models -       2
    Independent nodes -       3
       Boundary nodes -       7
          Total nodes -      10

Power Results

Total Power from time 0 to 8e-008
Average power consumed -> 2.290863e-004 watts
Max power 1.766991e-003 at time 3.1e-008
Min power 1.073915e-009 at time 1e-008


Parsing                         0.09 seconds
Setup                           0.03 seconds
DC operating point              0.01 seconds
Transient Analysis              0.04 seconds
Overhead                        1.14 seconds
-----------------------------------------
Total                           1.31 seconds

Simulation completed
```

5.3.2 PERFORMANCE EVALUATION METRICS OF 6T FULL ADDER USING XOR LOGIC

The second simulation report presents the same circuit structure as the first, with six MOSFETs, voltage sources, and identical node counts, but exhibits different power consumption characteristics. The average power consumed is approximately 0.124.4. mW, which is lower than the first simulation. The maximum power reaches 3.4.4.9 mW at 4.4.0.49 ns, while the minimum power drops to 0.23 nW at 100 ns. The total simulation time is reduced to 0.92 seconds, with parsing, setup, and transient analysis taking slightly less time than in the first report. The simulation successfully completes with improved efficiency.

```
General options:
        threads = 1

 Device and node counts:
              MOSFETs -       6
    MOSFET geometries -       2
      Voltage sources -       6
          Subcircuits -       0
    Model Definitions -       6
      Computed Models -       2
    Independent nodes -       3
       Boundary nodes -       7
          Total nodes -      10

Power Results

Total Power from time 0 to 8e-008
Average power consumed -> 1.259407e-004 watts
Max power 3.686092e-003 at time 6.04937e-008
Min power 2.322867e-010 at time 1e-008


Parsing                         0.07 seconds
Setup                           0.02 seconds
DC operating point              0.01 seconds
Transient Analysis              0.06 seconds
Overhead                        0.76 seconds
-----------------------------------------
Total                           0.92 seconds

Simulation completed
```

The circuits is implemented using pass transistor logic, Complementary Pass Transistor Logic and with the help of the logic first constructed the Ex-or gate circuit and Ex-nor gate circuit, then using MUX and the modules again obtained Sum and Carry. And observed the output. Tested by applying 1.2v and obtained simulations are verified through truth table. Then performed some analysis on Power consumption, Delay, Power Delay product and output noise, which then compared those with provided inference from the Table below.

Full adder design	**Parameters**				
	Technology	***Number of Transistors***	***Delay (ps)***	***Power Consumption (nW)***	***Power Delay Product (ps)*(nW)***
6T using 2T XOR	180nm	6	360	2.29*〖10〗^3	8244*〖10〗^4
6T using 2T XNOR	180nm	6	2*〖10〗^4	3.6*〖10〗^3	7200*〖10〗^4

TABLE 5.1 PERFORMANCE EVALUATION MENTORS

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

ADVANTAGES

Efficient implementation of a 6T full adder circuit using low-power 2T XOR-XNOR logic offers several advantages. The use of 2T XOR-XNOR gates significantly reduces dynamic and static power dissipation compared to conventional designs, making it ideal for energy-efficient applications. Reduced Transistor Count With fewer transistors (6T vs. traditional 28T or 10T adders), the circuit achieves a compact layout, reducing area and fabrication cost. High-Speed Operation simplified logic structure minimizes propagation delay, improving overall circuit speed and efficiency. Low Leakage Current optimized transistor configuration helps lower leakage power, which is crucial for sub-threshold and ultra-low-power applications. Scalability for VLSI Design compact design makes it highly suitable for large-scale integration in modern nano-meter CMOS technologies. Improved Reliability With fewer components, the probability of defects and failures is reduced, leading to increased robustness in real-world applications. Energy-Efficient Arithmetic Processing Ideal for battery-powered devices, IoT applications, and low-power computing systems requiring efficient arithmetic operations.

DISADVANTAGES

While implementing a 6T full adder using low-power 2T XOR-XNOR logic can improve efficiency and reduce power consumption, there are certain disadvantages to consider: Signal Degradation & Voltage Drops 2T XOR-XNOR logic relies on pass transistor logic, which can result in weaker output signals, leading to degraded voltage levels and potential logic errors in cascaded stages. Threshold Voltage Loss Due to the use of transmission gates or pass transistors, the circuit may suffer from threshold voltage (Vth) loss, reducing the drive strength and potentially requiring additional buffering. Leakage Power & Subthreshold Effects While dynamic power is reduced, leakage currents in deep submicron technologies can still contribute to power dissipation, especially in idle states.

Increased Delay reduced transistor count may introduce higher propagation delays, impacting circuit speed, especially in high-performance applications. Limited Driving Capability 2T XOR-XNOR gate has a weaker output drive compared to conventional static CMOS logic, requiring additional buffers when driving larger loads. Process Variations

Sensitivity – Due to the use of fewer transistors and pass-transistor logic, the design may be more sensitive to fabrication process variations, affecting robustness and reliability. Noise Margin Issues Since the voltage swing may not be full rail-to-rail, the noise margins are lower compared to conventional full CMOS implementations, making the circuit more susceptible to noise.

APPLICATIONS

The efficient implementation of a 6T full adder using low-power 2T XOR-XNOR logic has several applications in low-power and high-speed digital systems, particularly in energy-efficient computing. Some key applications include Low-Power Arithmetic Units Used in low-power ALUs (Arithmetic Logic Units) of microprocessors and digital signal processors (DSPs) to reduce overall power consumption. Suitable for multipliers and accumulators in power-constrained applications.

Battery-Powered Devices Ideal for mobile phones, smartwatches, and IoT devices, where power efficiency is crucial for longer battery life. Used in wearable electronics that require low-power processing for extended operation. Neuromorphic & AI Hardware Helps in the implementation of energy-efficient neural network accelerators for AI and machine learning applications. Used in approximate computing for deep learning inference tasks with minimal power consumption. Cryptographic & Security Circuits Used in lightweight cryptographic algorithms that require fast and energy-efficient arithmetic operations. Applied in hardware security modules (HSMs) and encryption circuits for secure communication. Biomedical and Implantable Devices Suitable for low-power biomedical sensors used in ECG, EEG, and implantable medical devices where power efficiency is critical. Used in neural signal processors for brain-machine interfaces (BMIs). Image and Signal Processing Found in low-power image processors for cameras and video compression systems. Used in speech processing and audio codecs for power-efficient sound processing. Wireless Sensor Networks (WSNs) & IoT Essential for low-power sensor nodes in IoT applications, enabling efficient data processing with minimal energy consumption. Used in edge computing devices that require power-efficient arithmetic operations. Quantum-Dot Cellular Automata (QCA) & Emerging Technologies Can be adapted to nanotechnology-based computing, including QCA and CNTFET-based circuits for ultra-low-power logic design.The 6T full adder with 2T XOR-XNOR logic is a promising solution for low-power, high-speed, and energy-efficient digital circuits, making it highly applicable in modern VLSI, IoT, AI, and biomedical applications.

CONCLUSION

The 6T full adder with 2T XOR-XNOR logic proposed the new design 2T XNOR-XOR gate circuit is based on the Pass Transistor Logic. The performances of this circuit have been compared to earlier designed XNOR-XOR gate delay, power dissipation and PDP. Also we proposed a new direct design for three-input XNOR-XOR function. The current work proposes the design of a 6T full adder using a novel 2T XNOR-XOR gate. The newly designed full adder process the merits of small delay, small Power-Delay product, and area saving due to lower transistor counts and special structures.

The efficient implementation of a 6T full adder using low-power 2T XOR-XNOR logic offers significant advantages in power-efficient and high-speed digital circuit design. Its reduced transistor count minimizes power consumption, making it highly suitable for battery-operated devices, IoT applications, AI accelerators, cryptographic circuits, biomedical devices, and energy-efficient computing systems.

However, challenges such as signal degradation, threshold voltage loss, and limited driving capability must be addressed for optimal performance. Despite these limitations, its application in low-power arithmetic units, neuromorphic computing, wireless sensor networks, and emerging nanoelectronics makes it a promising solution for future low-energy VLSI designs.

FUTURE SCOPE

The efficient implementation of a 6T full adder using low-power 2T XOR-XNOR logic holds significant potential for future advancements in low-power and high-speed computing. As semiconductor technology moves toward sub-10nm nodes and FinFET architectures, optimizing this design for next-generation fabrication processes can further enhance its power efficiency and performance. Additionally, its integration with emerging technologies like Quantum-Dot Cellular Automata (QCA), Carbon Nanotube FETs (CNTFETs), and Tunnel FETs (TFETs) can lead to even greater improvements in energy efficiency.

This design also has promising applications in neuromorphic computing, AI accelerators, and edge AI, enabling efficient arithmetic operations in low-power machine learning and deep learning systems. Furthermore, its potential use in biomedical implants, IoT devices, and flexible electronics highlights its relevance in future wearable and sensor-based applications.

However, challenges such as voltage degradation, noise sensitivity, and threshold voltage loss need to be addressed through advanced circuit techniques and hybrid logic designs. Despite these limitations, the 6T full adder with 2T XOR-XNOR logic remains a highly viable solution for energy-efficient VLSI design, ensuring its continued relevance in next-generation low-power digital systems.

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